REFO-SVM: Optimized PWM for Thermal Stress and Gate Switching Instability Mitigation in SiC MOSFETs

1st Amin Rezaeizadeh
Institute of Electric Power Systems
University of Applied Science Northwest Switzerland
amin.rezaeizadeh@fhnw.ch

2rd Silvia Mastellone
Institute of Electric Power Systems
University of Applied Science Northwest Switzerland
silvia.mastellone@fhnw.ch

***Abstract*—This paper proposes an optimized modulation mechanism for a two-level three-phase power electronics converter. The optimal switch selection is designed to address the two degradation factors in SiC MOSFETs: bond-wire lift-off and gate switching instability (GSI). The switching principle is based on space vector modulation (SVM) principle, however, in any voltage angle, one of the legs will be entirely either on or off to reduce the number of switching. Furthermore, the duty cycles are computed based on reducing the thermal stress of the switching devices. The simulation results are compared to three other SVM-based modulation techniques.**

***Index Terms*—Reliability, thermal stress, space vector modulation, SiC MOSFET, convex optimization**

I. INTRODUCTION

At the component level, the two types of reliability-critical components of a power electronics converter are semiconductor switching devices, such as MOSFETs, and electrolytic capacitors [1]. In automotive applications, SiC MOSFETs are switched up to 10^{11} times, whereas industrial applications range up to 3×10^{13} switching cycles [2]. As a result, this continuous switching mode plays a critical role in reliability and lifetime assessments. This switching operation is where a newly identified degradation mechanism—referred to as gate switching instability (GSI)—has been observed to occur [3]. Over time, this degradation mechanism causes a significant increase in the threshold voltage drift, ΔV_{th} [4], [5].

Thermal stress is another degradation factor of power switching devices, and a significant amount of research has been devoted to the electrical-thermal analysis and reliability assessment of these devices. The most frequent failure in a semiconductor switch is bond wire lift-off caused by stress cracks due to thermal cycling experienced by the device during operation. In this work, we propose a reliability- and efficiency-optimized space vector modulation, which we will refer to in short as **REFO-SVM**. This method incorporates the two degradation phenomena of semiconductor switches, i.e. the bond-wire stress and the GSI all in one control framework (see Fig. 1). The proposed method is benchmarked against the reliability-optimized modulation (ROSVM) [6], the conventional SVM and the minimized-switching SVM, the latter two being the built-in blocks in SIMULINK.

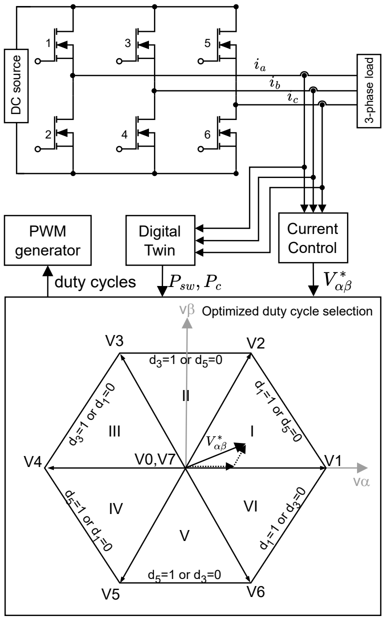

Fig. 1: Schematic of a two-level three-phase inverter controlled by the REFO-SVM scheme. This modulation method requires knowledge of the phase currents and the power loss values which are instantaneously computed by the digital twin.

II. SYSTEM DESCRIPTION

A. Principle of SVM

In traditional SVM, the target reference vector V^* is generated by rapidly switching between the two nearest active vectors and a zero vector (V_0 or V_7), as shown in Fig. 1 [7], [8]. Generally, this desired output voltage vector V^* can be represented as a time-weighted average of the space vectors V_i over the switching period T_{sw}. The SVM algorithm calculates the dwell times (T_i) for each vector so that the average output

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voltage $\bar{V}$ during the switching period T_{sw} approximates the required voltage as:

$$V^* \approx \bar{V} = \frac{1}{T_{sw}} \sum_{i=0}^{7} T_i V_i, \text{ subject to:} \sum_{i=0}^{7} T_i = T_{sw}, \qquad (1)$$

where T_{sw} denotes the switching period, and T_i is the dwelling time of the space vector V_i.

Equation (1) implies that there are multiple combinations of space vectors that can generate the same target vector V^*. This flexibility opens the possibility for optimization across various parameters. Conventional switching strategies typically rely on predefined rules; for example, by carefully selecting null vectors, switching patterns can be arranged to minimize switching losses, as demonstrated in the MATLAB/SIMULINK space vector modulation block, which serves as a benchmark in this study. However, existing methods generally do not address optimizing the thermal distribution across devices or consider the reliability of the switches, leaving potential improvements in these areas unexplored.

The averaged output vector can also be represented in terms of the duty cycles of the switches as follows:

$$\bar{V} = \frac{2}{3} V_{DC} \left(d_1 + d_3 e^{j\frac{2\pi}{3}} + d_5 e^{j\frac{4\pi}{3}} \right), \qquad (2)$$

where V_{DC} is the input DC voltage. The duty-cycles of the upper and the lower switches in each leg are complementary, implying that:

$$d_i + d_{i+1} = 1, \text{ for } \quad i = 1, 3, 5. \qquad (3)$$

B. Device model

Power semiconductors inherently dissipate energy due to their non-ideal characteristics, primarily through conduction losses and switching losses, while additional losses like leakage current-induced blocking losses are typically negligible [9]. Accurate calculation of these losses is essential for estimating junction temperature over time, a critical parameter for lifetime modeling. This study employs electrothermal models within PLECS to achieve these calculations. PLECS utilizes a look-up table approach or manufacturer-provided thermal descriptions to determine losses, relying on data derived from manufacturer datasheets or laboratory measurements [10]. In this context, pre-existing device models of SiC MOSFET (C3M0075120D) supplied by manufacturers are directly integrated for analysis. To determine device-level losses, the current and voltage loading at the converter level must be applied to the device-level models [11].

C. Lifetime models

Bond-wire degradation. In this work we use the lifetime model adopted by Semikron [12], to evaluate the semiconductor devices reliability. The number of cycles to failure, N_f, of the power switches due to thermal stress of the bond-wire is typically modeled by a Coffin-Manson lifetime model, such as the following one developed by Semikron:

$$N_f = A_0 . A_1^{\beta} . \Delta T^{\alpha - \beta} . \exp \frac{E_{\text{a}}}{\kappa_{\text{B}} T_j} . \frac{C + t_{on}{}^{\gamma}}{C + 2^{\gamma}} . k_{\text{thick}}, \qquad (4)$$

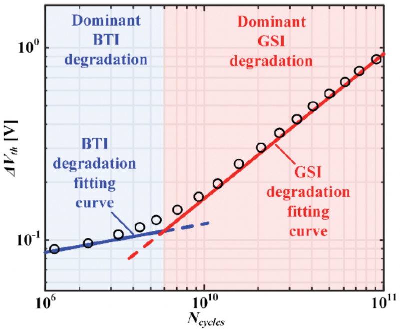

Fig. 2: The threshold voltage drift in a SiC MOSFET under gate switching stress (Courtesy of [4]).

where T_j and ΔT_j are, respectively, the average and magnitude of the junction temperature cycle, and t_{on} is the duration of the cycle. The remaining parameters are assumed to be constant and given as in [12].

Gate switching instability. The gate oxide reliability of SiC MOSFETs has been a subject of study for many years. The oxide/SiC interface was found to create drifts in device parameters like the threshold voltage (V_{th}), on-state resistance ($R_{DS(on)}$) and early lifetime fails. The drift in V_{th} from cycling depends on the number of switching cycles (N_{cycles}) and has been modeled in [4] as follows:

$$V_{th} = A_0 N_{cycles}^n, \qquad (5)$$

where A_0 is a constant parameter and where the exponent n depends on the number of switching cycles. Below about 10^7 number of cycles, the voltage drifts with a constant slope of $n \approx 0.16$. Above 10^8 cycles, the exponent n increases to 0.32. Figure 2 illustrates this change in the exponent as a result of different degradation mechanisms.

III. OPTIMIZED MODULATION SCHEME

Fig. 1 illustrates the switching control mechanism of the proposed modulation method. The phase currents are fed into the digital twin block where simulates the power losses and the thermal responses of the devices. The desired voltage reference vector $V_{\alpha\beta}^*$ together with the computed power losses from the digital twin are inputs to the modulation block. This block calculates the optimal selection of switches and their duty cycles with the aim of reducing thermal stress and GSI degradation.

Considering the fact that V_0 and V_7 are both zero vectors, for any given reference voltage sector there are at least two ways to generate the desired voltage without changing the state of a switch. For example, according to Fig. 1, if the reference voltage is located in sector 1, either switch 1 is conducting during the entire switching period (equivalently, switch 2 is open), or switch 5 is fully open and switch 6 is conducting. These two cases correspond to using the vectors $\{V_1, V_2, V_7\}$ and $\{V_1, V_2, V_0\}$, respectively, to generate the reference vector. The same approach may be applied to other voltage sectors.

For the two cases where a device is either on or off, the duty-cycles can be algebraically and uniquely determined from the complex equation (2).

This implementation not only reduces switching losses and therefore the junction temperature, but also results in a lower number of switching cycles which is beneficial for mitigating the GSI. Mathematically speaking, the following optimization problem is solved online to provide the optimized duty cycles for each voltage angle for every switching period:

$$\min_{d_i} \quad \sum_{1}^{6} P_i(t)^2 \tag{6a}$$

$$\begin{aligned} \text{s.t.} \quad & \text{power loss model} \\ & P_i = d_i P_{i,c} + P_{i,sw}, \ \text{for } i = 1, \ldots, 6 \qquad (6b) \\ & \text{The two options to generate } V^* \\ & d_i \in Set, \ \text{for } i = 1, \ldots, 6 \qquad (6c) \\ & \text{voltage reference constraint} \\ & V^* = \frac{2}{3} V_{DC} (d_1 + d_3 e^{j\frac{2\pi}{3}} + d_5 e^{j\frac{4\pi}{3}}), \qquad (6d) \end{aligned}$$

where d_i denotes the duty-cycle of device i, $P_{i,c}$ $P_{i,sw}$ are, respectively, the conduction loss and the switching loss of the device i obtained from the digital twin.

Note that the objective of the above optimization is to minimize the sum of the *squared* power losses which translate to temperature fluctuations in the semiconductor switches. Constraint (6b) addresses the impact of duty cycle on power loss, constraint (6c) selects the duty-cycles from the two given choices as described above. Finally, constraint (6d) guarantees generating the desired output voltage. It is worth mentioning that for devices where the duty cycle is set to either 0 or 1, the corresponding switching loss $P_{i,sw}$ will be set to zero in constraint (6b).

In summary, before each switching period T_{sw}, the power losses are computed by measuring the phase currents and applying the digital twin. The desired reference vector along with the power loss values are then used to pick the optimum duty cylces from the two given options. The duty-cycles that achieve the minimum cost are then used to generate the PWM signals for the gate drives. Algorithm 1 summarizes the modulation scheme.

Algorithm 1 The REFO-SVM Algorithm

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STEP 1: Capture $i_a(t), i_b(t), i_c(t)$, and $V^*_{\alpha\beta}(t)$
STEP 2: Compute the power loss for each device
STEP 3: Compute the duty-cycles according to (2)
STEP 4: Evaluate the cost value $\sum_{i=1}^{6} P_i^2$
STEP 5: Select the duty-cycles that result in the minimum cost value
STEP 6: generate and apply the PWM signals and go to STEP 1
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IV. SIMULATION RESULTS

This section presents the simulation results of the proposed REFO-SVM method applied to a two-level three-phase inverter with SiC MOSFETS (C2M0080120D) [13]. The simulation is implemented in SIMULINK using PLECS blockset for simulating the power losses and junction temperatures [14]. The simulation parameters are gathered in Table I and a detailed demonstration of the simulation setup is available in [15].

TABLE I: Simulation parameters.

Quantity	Value	Description
I_m	25A	Current magnitude
f_{sw}	10kHz	Switching frequency
f	50Hz	Signal frequency
V_{dc}	300V	DC-Voltage
m	0.8	Modulation index
R	0.3 Ω	Load resistance
L	15mH	Load inductance
R_θ	4°C/W	Thermal resistance of heat-sinks
C_θ	0.05J/°C	Thermal capacitance of heat-sinks
T_a	25°	Ambient temperature

The proposed REFO-SVM method is compared with three pulse patterns. One is based on the online quadratic programming (QP) optimization previously presented in [6]. The other two patterns are generated using the built-in 2-level SVPWM block in SIMULINK, denoted as SVM and SVM-P2 in here. The latter method generates patterns that the switching state of one switch remains unchanged throughout the entire switching period to minimize the switching losses.

Figure 3 illustrates the power loss profile of SiC MOSFET 1 (the upper switch of phase leg A) applying four modulation techniques. The figure also includes the phase A current waveform for reference. As shown, the conventional SVM and SVM-P2 methods result in peak power losses in the first half cycle, where the current reaches its maximum. In contrast, the RO-SVM and REFO-SVM approaches that employ the power loss models effectively reduce the magnitude of these peaks. Moreover, the REFO-SVM method achieves zero power loss during certain intervals of the switching period, which leads to a lower temperature rise and potentially lower thermal stress as shown in Fig. 4.

According to this figure, with the SVM method the switching device experiences the highest average temperature. This is expected since with the SVM method, all switches are activated without any feedback from the resulting power loss. On the other hand, the SVM-P2 results in the lowest average temperature which reflects its minimized switching loss pattern. However, the RO-SVM and REFO-SVM methods, which incorporate power loss models, yield average temperatures between those of SVM and SVM-P2. Both RO-SVM and REFO-SVM have more switching transitions than SVM-P2 and therefore result in higher average temperatures. However, due to their optimized duty cycles, the temperature rise is significantly lower than that observed with the SVM method. Furthermore, both methods show relatively low temperature swings, which is beneficial for the device reliability.

Thermal stress assessment. Fig. 6 shows a comparison of the four methods in terms of thermal stress and total power

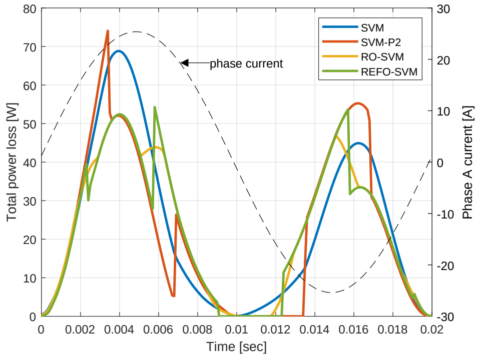

Fig. 3: Power loss profile of the SiC MOSFET number 1 (upper leg A) over one fundamental cycle.

loss. The thermal stress is calculated based on the bond-wire lift-off degradation model given in (4) and using the RainFlow counting algorithm to count the temperature cycles [16], [17]. As we can see, the SVM method exhibits the greatest thermal stress and power loss relative to other modulation methods. In contrast, the REFO-SVM method achieves the lowest values in both metrics, especially 50 times improvement in degradation compared to the SVM. Moreover, the REFO-SVM is, by design, optimized in terms of switch transitions. That is, as illustrated in Fig. 5, there are intervals within the fundamental cycle where the duty cycle is 0 or 1, i.e. no switch transition occurs which demonstrates its effectiveness in minimizing power loss as well as degradation due to thermal stress and gate switching instability.

GSI analysis. The fundamental cycle consists of 200 switching periods. Therefore, a power module operating with the standard SVM undergoes 200 switching cycles per fundamental cycle, whereas with the REFO-SVM, this number is reduced to 132—showing a 34% reduction in switching transitions. In other words, for the same operating duration, a converter using REFO-SVM can achieve up to 34% longer lifetime.

Employing the S–N curve model expressed in (5) for $N = 10^{11}$ switching cycles—which is a typical end-of-life threshold in automotive applications—leads to

$$\text{SVM:} \quad \Delta V_{th} \approx 1.43V, \tag{7}$$

$$\text{REFO-SVM:} \quad \Delta V_{th} \approx 1.29V, \tag{8}$$

which indicates 10% less drift in the threshold voltage V_{th}. This improvement in the threshold voltage drift also results in reduced power loss, which translates not only to higher efficiency but also to lower heat generation and consequently, reduced thermal stress.

V. CONCLUSION

This paper proposes an optimized modulation scheme for a two-level three-phase power electronics converter. The modulation technique, referred to as REFO-SVM, is based on space vector modulation scheme, however, the duty cycles are optimally computed to reduce the thermal stress. In this scheme, one switch and its corresponding complementary switch (either upper or lower) remain in a fixed state—either on or off—throughout the entire switching period. This mechanism is triply beneficial. First, it reduces the switching losses. Secondly, because the switching loss is reduced, the average junction temperature will also reduce leading to lower bond-wire stress. Third, with lower number of switching cycles, the threshold voltage of the device will experience less drift over time as a result of gate switching instability. A comparison of

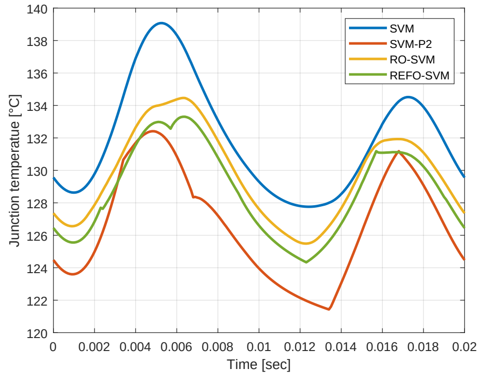

Fig. 4: Junction temperature profile of the SiC MOSFET number 1 (upper leg A) over one fundamental cycle.

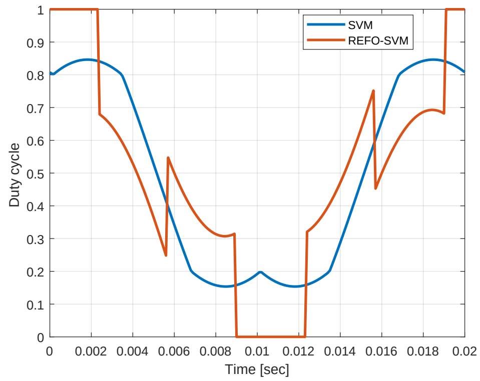

Fig. 5: Duty cycle profile of the device 1 over one fundamental cycle, using a conventional SVM method versus the REFO-SVM.

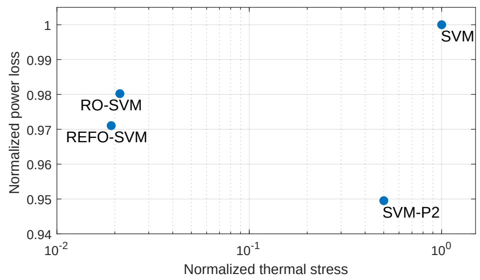

Fig. 6: Comparison of different modulation techniques in terms of power loss and thermal stress. The values are normalized with respect to those obtained using the SVM method.

the proposed REFO-SVM with the conventional SVM method shows 50 time improvement in thermal stress, as well as 25% improvement in threshold voltage drift.

REFERENCES

[1] E. Wolfgang, "Examples for failures in power electronics systems," *ECPE tutorial on reliability of power electronic systems, Nuremberg, Germany*, pp. 19–20, 2007.

[2] P. Salmen, M. W. Feil, K. Waschneck, H. Reisinger, G. Rescher, and T. Aichinger, "A new test procedure to realistically estimate end-of-life electrical parameter stability of sic mosfets in switching operation," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, 2021, pp. 1–7.

[3] P. Salmen, M. Feil, K. Waschneck, H. Reisinger, G. Rescher, I. Voss, M. Sievers, and T. Aichinger, "Gate-switching-stress test: Electrical parameter stability of sic mosfets in switching operation," *Microelectronics Reliability*, vol. 135, p. 114575, 2022. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271422000993

[4] J. R. Garcia-Mere, A. A. Gomez, J. Roig-Guitart, J. Rodriguez, and A. Rodriguez, "Aging modeling and simulation of the gate switching instability degradation in sic mosfets," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 653–658.

[5] M. W. Feil, K. Waschneck, H. Reisinger, J. Berens, T. Aichinger, S. Prigann, G. Pobegen, P. Salmen, G. Rescher, D. Waldhoer, A. Vasilev, W. Gustin, M. Waltl, and T. Grasser, "Gate switching instability in silicon carbide mosfets—part i: Experimental," *IEEE Transactions on Electron Devices*, vol. 71, no. 7, pp. 4210–4217, 2024.

[6] A. Rezaeizadeh and S. Mastellone, "Reliability-optimized space vector modulation (ro-svm) for semiconductors lifetime enhancement," in *PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2024, pp. 1681–1687.

[7] Z. Yu, "Space-vector pwm with tms320c24x/f24x using hardware and software determined switching patterns," in *Texas Instruments Application Report SPRA524*, 1999, pp. 24–28. [Online]. Available: https://api.semanticscholar.org/CorpusID:62064461

[8] P. Handley and J. Boys, "Space vector modulation: an engineering review," in *1990 Fourth International Conference on Power Electronics and Variable-Speed Drives (Conf. Publ. No. 324)*, 1990, pp. 87–91.

[9] PLECS, *PLECS User Manual*, PLEXIM GmbH, 2024, https://www.plexim.com/sites/default/files/plecsmanual.pdf.

[10] Y. Kishor and R. Patel, "Performance comparison and thermal analysis of recently introduced high gain converters," in *2022 IEEE Region 10 Symposium (TENSYMP)*, 2022, pp. 1–6.

[11] P. Górecki and D. Wojciechowski, "Accurate computation of igbt junction temperature in plecs," *IEEE Transactions on Electron Devices*, vol. 67, no. 7, pp. 2865–2871, 2020.

[12] A. Wintrich and U. Scheuermann, "Power cycle model for IGBT product lines," Semikron Danfoss, Nuremberg, Germany, Application Note AN21-001, 2021.

[13] *Silicon Carbide Power MOSFET C2M^{TM} MOSFET Technology N-Channel Enhancement Mode*, Wolfspeed, 11 2023, rev. 5.

[14] *User Manual of PLECS Blockset Version 4.8*, February 2024, https://www.plexim.com/sites/default/files/plecsmanual.pdf.

[15] A. Rezaeizadeh, "Power electronics modulation using convex optimization (cvxgen)," https://www.youtube.com/watch?v=zVVHNsL2pk8, 2025, accessed: May 15, 2025.

[16] E. ASTM *et al.*, "Standard practices for cycle counting in fatigue analysis," *Standard Practices for Cycle Counting in Fatigue Analysis*, 2011.

[17] A. Czechowski and A. Lenk, "Miner's rule in mechanical tests of electronic parts," *IEEE Transactions on Reliability*, vol. R-27, no. 3, pp. 183–190, 1978.