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# Silicon Carbide Potential for Railway Traction Applications: Efficiency, Loadability, Life Cycle Energy Analysis, and Cost Assessment Comparison to Si-Based Inverter Topologies

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**Abstract**

Silicon carbide (SiC) power devices are emerging as an alternative for electrical transportation systems to improve energy efficiency, reduce carbon emissions, increase power density, and enable long-term cost savings throughout the product life cycle. Thus, a fair comparison with state-of-the-art Silicon (Si) technology is required to justify the productization of SiC devices. This work performs a systematic investigation of both technologies at the device and system levels for distinct power module voltage classes (3.3 and 6.5 kV) and circuit topologies. Initially, experimental characterization of state-of-the-art power modules is performed, followed by energy efficiency characterizations at the power converter level. Then, an electrothermal simulation model was built and validated based on experimental results. Accurate system simulations of commercial two- and three-level traction topologies were developed, focusing on efficiency over the entire load range, loadability, potential energy savings under realistic train drive cycles, and a financial comparison of inverter prices per kW. SiC exhibits lower loadability degradation at high switching frequencies (>500 Hz) than Si technology. Energy-saving potentials of 40–70% in the traction inverter with a guaranteed return on investment during the converter's lifetime are achieved by substituting Si with SiC inverters. In addition, massive energy savings of up to 200 MWh per inverter lifetime can effectively reduce the carbon footprint of railway systems (up to ~76 t $CO_2$-eq saved during the inverter lifetime). This paper provides essential information for distinct stakeholders to support the decision-making process and design considerations for future railway power conversion technologies.

**Keywords:** silicon carbide MOSFET; railway traction; life cycle energy assessment (LCEA); silicon IGBT; power semiconductor module; power electronics; cost analysis



Academic Editor: Frédérique Ducroquet

Received: 6 February 2026
Revised: 4 April 2026
Accepted: 15 April 2026
Published: 27 April 2026



## 1. Introduction

Silicon carbide (SiC) devices are emerging as a key enabler in power electronics, enabling performance levels that are not possible with mainstream Si devices [1]. A well-known improvement enabled by SiC technology is higher conversion efficiency, which is essential to reduce the technology's carbon dioxide footprint [2]. In addition, SiC enables higher efficiencies at higher switching frequencies, supporting high-power-density systems with reduced size and weight [1]. Several commercial low-voltage (LV) applications (<1.5 kV DC) have already introduced SiC into their topologies, with Electric Vehicle (EV)

traction and Photovoltaic (PV) as the main industry drivers [3,4]. SiC-based medium-voltage (MV) applications (>1.5 kV DC) are expected to grow as the MV supply chain matures over time. However, a challenge in SiC productization is the device's higher initial cost compared to Si technology [3], which forces engineers to justify these costs through reduced system size or long-term cost savings, e.g., that enables lower Total Cost of Ownership (TCO).

Rail traction is a particularly demanding application for MV power semiconductors because traction inverters must combine high reliability and long service life (typically decades) with high efficiency over highly dynamic duty cycles. In practice, traction operation is frequently dominated by partial-load operation during cruising and coasting, while acceleration and regenerative braking impose short periods of high current and elevated junction temperature. In addition, insulation stress and electromagnetic compatibility constraints become critical in the presence of long motor cables, making $dv/dt$ a system-level design driver and not merely a device-level metric. These characteristics make railway traction a relevant benchmark to quantify not only device losses, but also converter efficiency, loadability, lifetime energy savings, and economic payback under realistic mission profiles.

Investigating the performance of 3.3 kV SiC modules in railway applications is essential for an optimal design [5]. The complete understanding of the impacts of this emerging technology in railway systems directly affects the converter system as part of the overall traction chain, jointly with the motor, transformer, filters, cooling system, and train car itself. Some affected Key Performance Indexes (KPIs) are energy losses, efficiency, reliability, power density, costs, design complexity, protection, robustness, and lifetime. These parameters should be evaluated individually for each component from a system-level perspective, considering the design interdependencies between components and the system. However, the overall complexity of the whole system imposes a challenging task for engineers due to the enormous amount of resources required to perform tests in such a complex system. On top of that, the use of MV devices makes the challenge even harder due to the complex and expensive infrastructure required, as well as the reduced supply chain available for such new devices. Consequently, most of the research is performed in companies, with the prototypes designed mainly by industrial enterprises [6] due to the infrastructure available.

Figure 1A shows a block diagram of a traction circuit configuration fed by the catenary wires, composed of a front-end circuit that converts AC power to DC, followed by the traction inverter (DC-to-AC conversion) that controls the motors. When the catenary is DC-powered, the front-end circuit is not required. The focus of the research in this paper is the traction inverter, which will be composed of LinPak power modules with IGBT half-bridges or SiC MOSFET half-bridges. Figure 1B shows the timeline of events on 3.3 kV SiC technology for railway traction.

In 2015, Mitsubishi [7] reported the first all-SiC traction inverter. The power module characterization was disclosed, but the manuscript did not focus on the converter performance. In 2018, Bombardier with KTH [8] demonstrated the reliable operation of a SiC-based inverter operating in the Stockholm metro. The results presented the operation in an actual drive cycle while monitoring the heatsink temperature. In 2020, the Central Japan Railway Company [9] showed the development of a SiC traction system used in Shinkansen trains, focusing on the new cooling and motor design improvements allowed by the SiC technology.

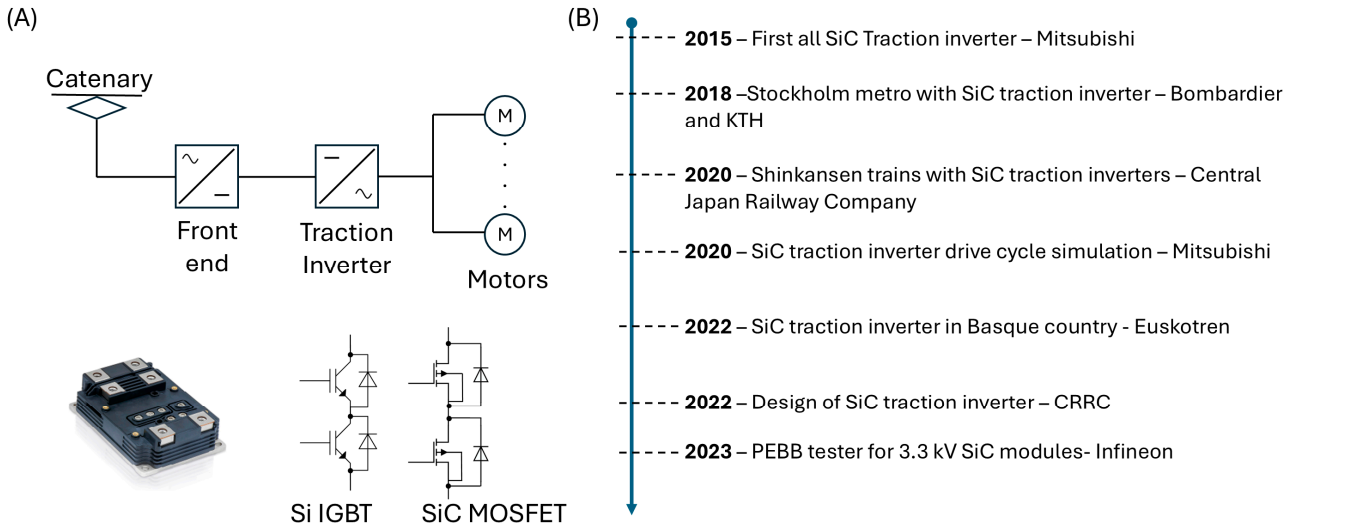



**Figure 1.** (**A**) Generic block diagram of a traction main circuit configuration. A photo of a 3.3 kV LinPak module is presented with the possible internal semiconductor configurations (Si IGBT half-bridge and SiC MOSFET half-bridge). (**B**) Chronological progression of research on 3.3 kV SiC technology for railway traction [7–13].

Further, in 2020, Mitsubishi [10] demonstrated a simplified drive cycle simulation comparison between Si and SiC modules, comparing power losses and providing the financial savings of the SiC technology over Si due to the energy cost reduction. More recently, in 2022, Euskotren [11] demonstrated a full-SiC traction converter, focusing on the characterized efficiency curves and converter size (weight) optimization compared to a Si IGBT converter. In 2022, the company CRRC [12] also demonstrated the design of a SiC inverter with a particular focus on the busbar, short circuit protection and $dv/dt$ filter. Finally, in 2023, Infineon [13] showed for the first time a power electronic building block (PEBB) tester to provide a systematic loss evaluation of the 3.3 kV SiC modules.

These investigations demonstrate the technology's potential in improving overall system efficiency, power density, cost savings, and loss reduction. Nevertheless, each publication focused on different aspects of the design. Furthermore, a systematic investigation of distinct design conditions and operation points is still missing to build a coherent understanding of the SiC impact on railway systems.

Some key points that require further investigation are the energy losses of SiC compared to Si modules under similar rating and packaging characteristics across the full load current range and for distinct switching frequencies. Such characterization is essential to investigate the SiC behavior under partial-load conditions, where the SiC unipolar conduction mechanism behavior presents outstanding performance compared to the bipolar IGBT technology. Furthermore, it is in the partial-load regime that traction inverters operate most of the time [6,8,9], requiring further investigation. The systematic investigation of two-level and three-level topologies with SiC technology in terms of nominal power, loadability, efficiency, and costs compared to equivalent Si IGBT converters is also required. The investigation must also encompass evaluation under typical railway drive cycles to characterize energy loss and costs during the entire converter lifetime as well as performance under distinct drive cycle conditions. Such analysis would provide a deeper understanding of the system operation in the final application.

Finally, the financial assessment of the SiC technology is vital for deployment decisions. In order to provide a fair financial comparison between Si and SiC-based railway converters, ideally, the investigation should be performed considering the entire converter lifetime,

where potential SiC cost savings in the use-phase due to lower losses can be included in the comparison, and not only the initial converter price.

This manuscript aims to evaluate railway traction based on MV SiC power semiconductors. A systematic evaluation and comparison with Si technology is performed, focusing on the main industrial topologies. It is essential to mention that this work blends the analysis of distinct MV classes (3.3 and 6.5 kV), device technologies (Si and SiC), and circuit topologies (two-level and three-level) based on extensive experimental data, provided in this manuscript, of state-of-the-art power modules that are not yet widely commercially available. Such a dataset is difficult to obtain in one single paper with systematic comparison under fair and equal experimental conditions due to the limited access to such technologies. The focus is to provide analyses on a vast range of typical railway traction design considerations and operating conditions to enable a complete and systematic comparison that supports optimized design decisions. Furthermore, this paper provides a common theoretical and experimental baseline for fairly comparing distinct design possibilities for a railway traction system, without requiring data gathering from separate works that present distinct methodologies, which makes it hard to benchmark the several design possibilities. The main contributions of this manuscript are described below:

- Design and implementation of a back-to-back (B2B) test bench power converter to evaluate Si and SiC 3.3 and 6.5 kV power modules with accurate power loss characterization via calorimetric and electrical methods.
- Characterization of Si IGBT 3.3 kV/450 A, Si IGBT 6.5 kV/300 A, and SiC MOSFET 3.3 kV/500 A power modules tested in the same system, thus allowing a direct performance comparison.
- Electrothermal modeling of two-level voltage source converter (VSC) and three-level active neutral-point-clamped (ANPC) converter with validation from experimental results.
- Systematic evaluation of the efficiency, power losses, and loadability of Si and SiC-based power inverters for railway traction.
- Life cycle energy savings of SiC-based railway inverters compared to Si technology are considered over the entire product lifetime, with use-phase evaluation under realistic railway drive cycles.
- Financial comparison between different power converter topologies and technologies.

The remainder of the paper is organized as follows: Sections 2 and 3 describe the B2B test bench and the static/dynamic characterization of the investigated power modules as well as the converter performance assessment; Section 4 details the validated electrothermal model; Section 5 translates device-level results into inverter- and mission-level metrics (efficiency, loadability, drive-cycle energy, lifetime $CO_2$-eq, and payback time).

## 2. Test-Bed Setup

### *2.1. Single-Phase Two-Level Back-to-Back (B2B) Converter*

One traditional technique to characterize high-power converter losses is based on the opposition method [14]. This technique connects two identical systems back-to-back, allowing high power to circulate between the systems with a low-power electrical source and without dissipative loads. The physical principle is demonstrated in Figure 2A, where the power source only provides the power losses ($P_{System1}$ + $P_{System2}$ + $P_L$) dominated by semiconductor losses from system 1 ($P_{System1}$) and system 2 ($P_{System2}$) and inductor losses ($P_L$). At the same time, a high power ($P_{cir}$) circulates between the systems. This is possible because there is no passive load dissipating high active power. Consequently, the power supplied by the source is low when the system operates at nominal conditions, significantly reducing the facility requirements. This method can be used for any reversible power

electronic topology [14], and it is the state-of-the-art method employed in the industry for high-power MV converter characterization [15]. Figure 2C shows the designed converter test-bed setup.

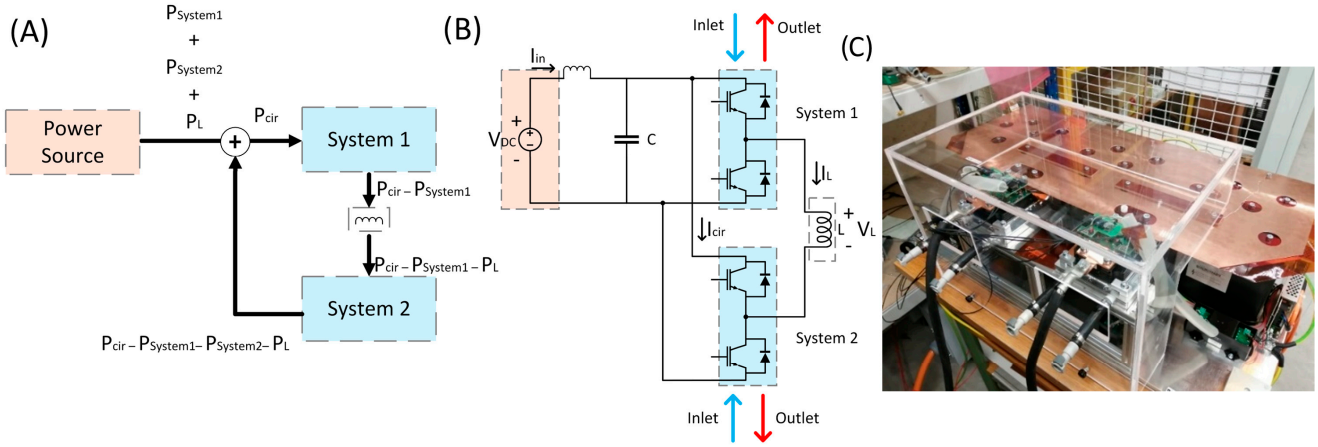



**Figure 2.** (**A**) Opposition method principle. (**B**) Circuit schematic of half-bridge converter characterization tester. (**C**) B2B converter.

Our system comprises two half-bridge legs, forming a traditional H-bridge inverter (Figure 2B). The first leg (System 1) is the device under test (DUT), and the second leg (System 2) acts as an active load, modulating the AC voltage at 50 Hz. An inductor is connected to limit the current due to the differential voltage between the H-bridge legs. By using a sinusoidal pulse-width-modulation (SPWM) control, it is possible to adjust the fundamental voltage vectors of the two legs to control the magnitude and phase angle of the voltage across the inductor L ($V_L$). Such control is performed by changing the modulation factors (M1, M2) that are responsible for the amplitude voltage control of each leg and the phase shift (θ) between the fundamental voltage outputs of each leg. With the phase shift angle and modulation indexes, it is also possible to control the load power factor, allowing investigation of converter operation under different power factors [16]. In order to characterize the inverter losses under a specified operating condition, the inductor voltage ($V_L$) is selected to achieve the desired inductor current. Analytical power relations for the B2B method are described in [16].

In this work, three state-of-the-art LinPak power modules are investigated: Si IGBT 3.3 kV/450 A [17], Si IGBT 6.5 kV/300 A [18], and SiC MOSFET 3.3 kV/500 A [19]. Such modules are based on the half-bridge configuration, with high and low side switches [6]. Thus, the tester should be able to handle distinct DC link voltage ($V_{DC}$) and load currents ($I_L$). For an inverter designed with 3.3 kV/500 A or 6.5 kV/300 A rated power modules, the nominal circulated power of about 200–250 kVA can be easily achieved with the B2B method. Furthermore, the switching frequency can be changed to investigate the losses under a range of operational frequencies. Table 1 shows the B2B converter design requirements to test the desired power modules. The voltages are typical of railway traction commercial inverters. In addition, the DC link voltage may not be fixed during train operation due to grid variations caused by several trains accelerating and braking, resulting in a certain range of operational DC link values. The testing system was designed to operate at a maximum load current of about 60–70% of the module nominal current, a realistic condition in real converters to guarantee long-term reliability during operation [20] due to the long lifetime required in traction inverters (~25–30 years) [21]. The included inductor in series with the power supply (Figure 2B) aims to improve the harmonic content of $I_{in}$ and thereby improve the accuracy of the power loss measurement. Such an inductor presents negligible losses due to the low power supply current [14].

**Table 1.** B2B converter requirements.

| | **3.3 kV/450 A Si IGBT Converter** | **6.5 kV/300 A Si IGBT Converter** | **3.3 kV/500 A SiC MOSFET Converter** |
|---|---|---|---|
| DC link voltage ($V_{DC}$) | 1.5 or 1.8 kV | 3 or 3.6 kV | 1.5 or 1.8 kV |
| Switching frequency ($f_s$) | 500–1250 Hz | 500 Hz | 500–3000 Hz |
| Inductor current range ($I_L$) | 0–300 $A_{rms}$ | 0–210 $A_{rms}$ | 0–300 $A_{rms}$ |
| Circulated power ($P_{cir}$) | ~0–160 kW | ~0–230 kW | ~0–160 kW |
| Modul. factor (both legs) (M) | 0.9 | 0.9 | 0.9 |
| Fundamental frequency (f) | 50 Hz | 50 Hz | 50 Hz |
| Current THD at 500 Hz | ~12% | ~12% | ~12% |

### *2.2. Power Losses Characterization—Calorimetric and Opposition Methods*

The main goal is to determine the power module's losses and converter efficiency. Two methods are used to characterize the H-bridge converter losses. The calorimetric (or thermal) and opposition (or electrical) methods are detailed below. All measurements are performed at steady state under continuous operation to avoid any transient behavior.

(1) The first characterization is based on the water flow exchanger method (calorimetric method) [14]. Here, the semiconductor power losses can be directly obtained using a water-cooled system for the power modules. The principle is based on the heat exchange between the coolant and the semiconductors. Therefore, the coolant flow rate and the inlet and outlet temperature difference must be properly measured for each power converter system as shown in Figure 2B. Equation (1) shows the relation between semiconductor power losses, the input and output temperature difference and the coolant flow rate [14].

$$P_{lossleg} = \Delta T * c * \rho * Q \quad (1)$$

where $P_{lossleg}$ is the semiconductor losses (W), $\Delta T$ is the inlet and outlet coolant temperature difference (K), c is the coolant-specific heat capacity (J/kg.K), $\rho$ is the coolant mass density (kg/$m^3$), and Q is the coolant volume flow rate ($m^3$/s).

(2) The second characterization is based on the opposition method [14]. Here, we electrically measure the voltage and currents using a power analyzer (Model: Hioki PW8001, HIOKI E.E. CORPORATION, Ueda City, Japan). The total system losses are measured directly from the power supply. In order to obtain the semiconductor power losses, the inductor losses must also be characterized. Therefore, we measure the inductor losses ($P_L = \left(\frac{1}{T}\right)\int_t^{t+T} V_L(t) * I_L(t)dt$), system total power losses ($P_{losstotal} = \left(\frac{1}{T}\right)\int_t^{t+T} V_{DC}(t) * I_{in}(t)dt$) and circulated power ($P_{cir} = \left(\frac{1}{T}\right)\int_t^{t+T} V_{DC}(t) * I_{cir}(t)dt$). The measuring points are indicated in Figure 2B.

The converter efficiency ($\eta$) can be obtained for the back-to-back converter [22], as shown in Equation (2). We consider the efficiency of the whole B2B converter (2 half-bridge legs), and not only one individual leg's efficiency. The inductor losses were subtracted in the analysis since the focus are on the semiconductors:

$$\eta = 1 - \frac{P_{loss}}{P_{cir}} \quad (2)$$

where $P_{loss}$ ($P_{loss} = P_{losstotal} - P_L$) is the semiconductor losses from both half-bridge legs (W).

Both methods constitute state-of-the-art power losses measurement approached in MV power converters. Their results will be compared to provide a consistent and reliable analysis. It is important to mention that to characterize the converter

efficiency (Equation (2)), the electrical method is required to measure the circulated power ($P_{cir}$) since the thermal method can only characterize the semiconductor losses.

## 3. Power Module and Converter Characterization

The device characterization results in this section are used for two purposes: to establish fair, experimentally grounded comparisons between Si and SiC power modules under the same packaging and test conditions; and to parameterize the electrothermal inverter models used later to quantify system-level consequences (efficiency, loadability and lifetime energy/cost impact) under realistic railway operating profiles.

### *3.1. Static Characterization*

The SiC power module was characterized by a Keysight B1505A Power Device Analyzer (Keysight Technologies, Inc., Santa Rosa, CA, USA) at 25 and 125 °C junction temperatures. Figure 3A compares the forward curves of the SiC MOSFET and Si IGBT power modules. At 25 °C junction temperature, the SiC MOSFET presents lower on-state losses across the whole current range up to the nominal current of 500 A. At lower currents, the SiC on-state losses are much lower than those of the Si IGBT due to the unipolar conduction mechanism, which creates a linear behavior over the full load current range. On the other hand, the Si IGBT presents a bipolar conduction mechanism with a knee close to 0.7 V that increases the on-state losses in the partial-load regime. At higher junction temperatures (125 °C), the SiC MOSFET shows lower losses up to around 300 A. For higher currents (>300 A at 125 °C), the Si IGBT presents lower on-state losses. These results demonstrate that SiC MOSFETs are advantageous at partial-load regimes, mainly at lower junction temperatures. This is a typical characteristic encountered in railway traction inverters, where the inverter usually operates at partial-load conditions.

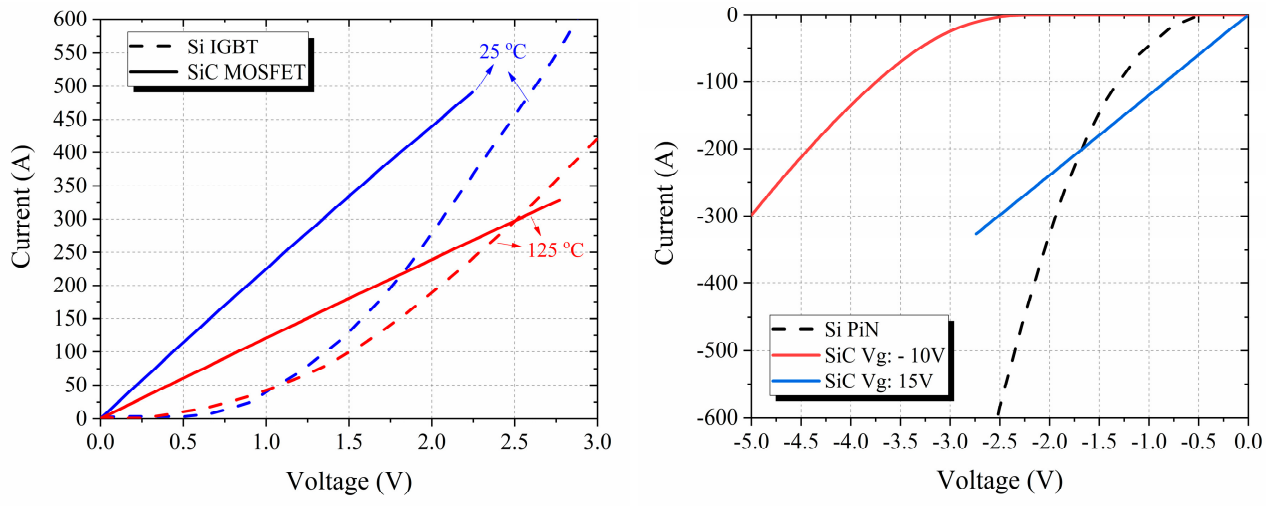



**Figure 3.** (**A**) Forward curves at 25 and 125 °C junction temperatures for the 3.3 kV/450 A Si IGBT and 3.3 kV/500 A SiC MOSFET. At 25 °C junction temperature, the SiC MOSFET presents lower on-state losses in the whole current range of interest. At 125 °C, the SiC MOSFET device presents lower losses up to around 300 A; (**B**) Forward curves (third quadrant operation) at 125 °C for the 3.3 kV/450 A Si PiN antiparallel diode and 3.3 kV/500 A SiC MOSFET at gate voltages of −10 V (intrinsic body diode) and +15 V. The SiC MOSFET (Vg: +15 V) presents lower on-state losses than the Si diode up to 200 A.

Figure 3B compares the third quadrant operation of the SiC MOSFET and Si PiN antiparallel diode at 125 °C junction temperature. The SiC MOSFET presents lower on-state

losses than the Si diode up to 200 A. Not shown here, at 25 °C junction temperature, the SiC body diode presents lower on-state losses up to 500 A. Figure 3B also indicates the SiC body diode when the gate voltage is −10 V. Such a case is important during the half-bridge leg dead time when conduction through this diode may occur. At this conduction mode, the diode presents very high on-state losses. However, this case happens only during a short time in the dead-time period, and is therefore typically less critical as in the case of a +15 V gate voltage. In general, the third quadrant operation presents similar behavior to the first quadrant, with improved SiC performance in the partial-load regime.

### *3.2. Dynamic Characterization*

The switching characterization was performed using a double pulse test configuration [23] with a single power module assembled. The double pulse test configuration was adapted from the converter setup in Section 2.1, using the same DC link capacitors and busbar. The voltage was measured with a 350 MHz voltage probe, and the current with a CWT Mini50 HF—50 MHz Rogowski coil. A 500 MHz oscilloscope (Keysight MSOX3054T—500 MHz, 5 GSa/s, Keysight Technologies, Inc., Santa Rosa, CA, USA) was used for data acquisition. Figure 4 shows SiC MOSFET switching curves at a junction temperature of 125 °C, a 1.5 kV DC link voltage, 405 A switched current and gate resistance of 2.4 Ω. A low overvoltage peak of around 2 kV indicates an optimal power loop design with a low stray inductance loop (~30 nH). Typical oscillations caused by the fast switching are observed due to interaction of the output device capacitance and power loop inductance. The device presented a $dv/dt$ of ~38 V/ns at turn-off and ~15 V/ns at turn-on. The $di/dt$ is ~6 A/ns at turn-off and ~4 A/ns at turn-on. Such values show an ultra-fast switching compared to $dv/dt$ and $di/dt$ literature values of similar rated SiC power modules, e.g., ~21 V/ns and ~7 A/ns [24], and ~10.6 V/ns and ~3.69 A/ns [25].

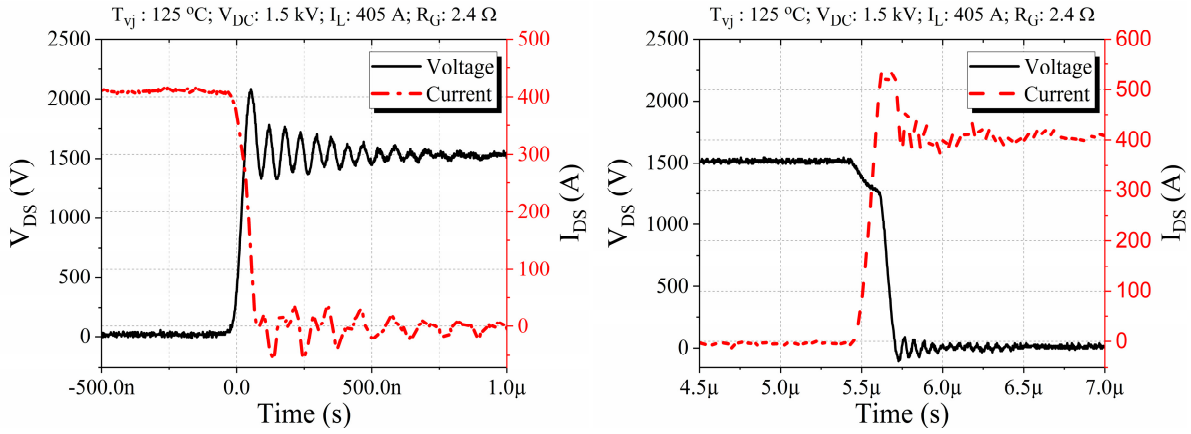



**Figure 4.** Turn-off (**A**) and turn-on (**B**) at 125 °C, 1.5 kV, 405 A, $R_G$: 2.4 Ω for the 3.3 kV/500 A SiC MOSFET module.

Figure 5 compares the SiC MOSFET and Si IGBT switching losses at 125 °C junction temperature. The results from this figure are obtained from several experimental curves similar to the ones presented in Figure 4 by performing sweeps in the switched current for the SiC MOSFET and IGBT in the double pulse setup. From the switching curves, the power is computed and integrated to obtain the switching losses for each switched current [23]. Approximately 6.6 times smaller turn-on losses and 30 times smaller turn-off losses at 400 A are observed compared to Si technology. Another characteristic observed is that the predominant switching losses for SiC MOSFETs are the turn-on losses, with the turn-off losses being significantly reduced, in agreement with previous works [24,25].

Not shown here are the SiC MOSFET losses at 25 °C, which are almost identical to the losses at high temperatures, presenting an almost temperature-independent behavior. The reverse recovery losses of the SiC body diode presented values smaller than 15 mJ for the whole current range, remaining negligible compared to the total switching losses. Such characteristics show the great advantage of SiC MOSFETs in enabling highly efficient high-frequency operation that can improve power converter density.

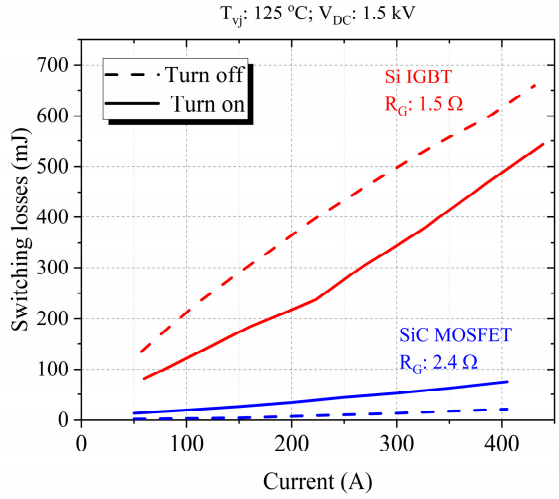
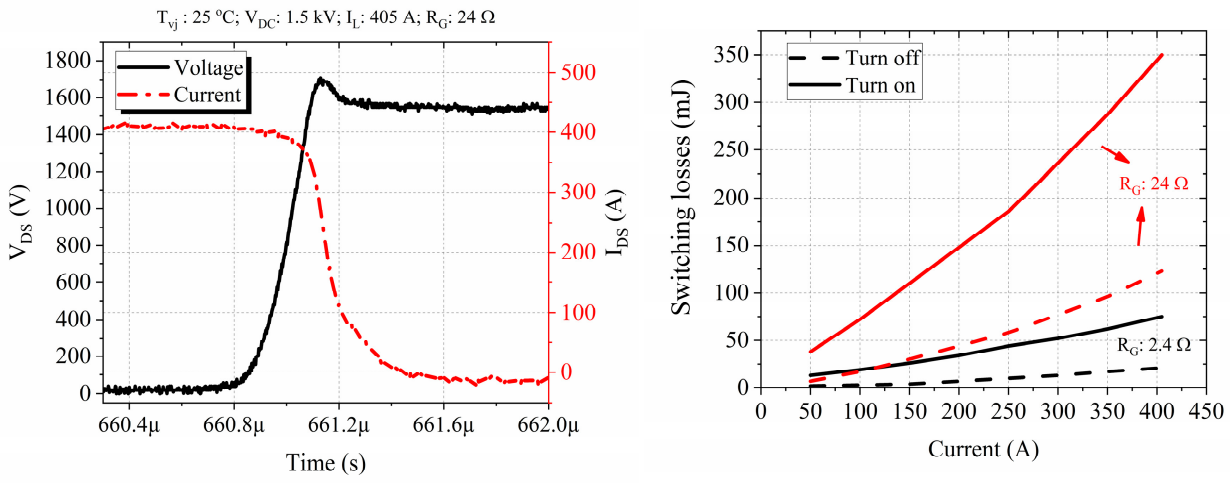



**Figure 5.** Switching losses of the 3.3 kV/500 A SiC MOSFET module at 125 °C, $V_{DC}$: 1.5 kV, compared to the Si IGBT 3.3 kV/450 A module. The Si IGBT losses were measured at 1.8 kV and linearly scaled down to 1.5 kV.

Investigating the gate resistance impact on SiC MOSFET switching curves is essential due to EMC issues that may arise due to the fast voltage variation. Such a high $dv/dt$ rate is critical when these power modules are used in a traction inverters connected to a motor with long cables. Depending on the cable length that connects the inverter output to the motor and the $dv/dt$, reflecting waves may arise, creating overvoltages in the motor terminals [26]. A $dv/dt$ smaller than ~6 V/ns should be targeted to avoid insulation lifetime degradation [27]. One possible way to mitigate this issue is to reduce the device switching speed using higher gate resistors or implementing external Miller capacitances [27]. Figure 6A shows the turn-off curve of a SiC MOSFET module at a gate resistance of 24 Ω. Due to the higher gate resistance, a slower $dv/dt$ of around 7 V/ns is obtained. Reduced overvoltage of approximately ~200 V (~1.7 kV peak voltage) and no oscillations are observed due to the slower switching. Further consequences of this speed reduction are indicated in Figure 6B where the losses increase compared to the gate resistance of 2.4 Ω is shown. Values up to 350 mJ are obtained compared to the low gate resistance case of 75 mJ. Even if the maximum $dv/dt$ of ~7 V/ns is still slightly higher than the limit of 6 V/ns (further increases in gate resistance would be required), this will be investigated as a condition that may not require additional output $dv/dt$ filters in the converter depending on the cable length from the motor to the inverter. It is expected that in the future, motor insulation may be able to handle up to 15 V/ns [27]. The Si IGBT modules present a switching speed lower than 6 V/ns, being in the range of 4 V/ns for the 3.3 kV modules and even lower for the 6.5 kV module tested with the recommended gate resistances of 1.5 and 7.5 Ω, respectively.




(**A**) (**B**)

**Figure 6.** (**A**) Turn-off at 25 °C, 1.5 kV, 405 A, $R_G$: 24 Ω for the 3.3 kV/500 A SiC MOSFET module. A *dv*/*dt* of around 7 V/ns is obtained with maximum overvoltage of 200 V (peak at 1.7 kV) and no oscillations. (**B**) Switching losses comparison of the 3.3 kV/500 A SiC MOSFET module at 25 °C, V: 1.5 kV, for gate resistances ($R_G$) of 2.4 and 24 Ω. Values up to 350 mJ are obtained compared to the low gate resistance case of 75 mJ.

### *3.3. Losses and Efficiency Characterization*

This section focuses on the power losses and efficiency characterization of the Si and SiC power modules operating in a B2B configuration. Figure 7 shows typical curves from one test at 270 $A_{rms}$ inductor current, circulated power of 120 kW, with the inductor current presenting a sinusoidal current behavior with a THD of 10%, the DC link voltage has a ripple smaller than 10% as predicted in the design phase and all curves are in agreement with the expected behavior.

Figure 8A–C show the semiconductor power loss characterization (thermal and electrical methods from Section 2.2) from the 3.3 kV Si IGBT-based converter for four switching frequencies in a current load range of up to 300 $A_{rms}$, the 3.3 kV SiC MOSFET-based converter ($R_G$ = 24 Ω) at 1500 Hz in a current load range of up to 300 $A_{rms}$, and the 6.5 kV Si IGBT-based converter at 500 Hz and two DC link voltages in a current load range of up to 210 $A_{rms}$, respectively. The electrical and calorimetric characterization methods show similar power losses, proving the equivalence of the methods and the high accuracy of the test-bed setup.

A comparison between the 3.3 kV Si and SiC-based power converter systems is presented in Figure 9. The SiC technology presents significantly lower power losses, reaching a maximum value of around 1500 W at a high switching frequency of 3000 Hz. On the other hand, the Si IGBT technology presented up to 2200 W (~46% higher) power loss values than the SiC system operating at a six times lower switching frequency of 500 Hz at ~280 $A_{rms}$. Another characteristic is the switching frequency's strong influence on the Si technology's power losses, with the losses almost doubling at 300 $A_{rms}$ from 500 to 1250 Hz. On the other hand, the SiC technology presented a less significant increase in the losses (~800 to ~1300 W) at 280 $A_{rms}$ with a larger switching frequency variation from 500 up to 3000 Hz. These trends are consistent with the operating conditions demonstrated in Section 3.2, where the SiC technology presents an optimized design for low switching losses. These comparisons were performed with the Si IGBT system operating at a slightly higher DC link voltage of 1.8 kV compared to the 1.5 kV of the SiC system. Consequently, the Si IGBT-based system would have slightly lower losses at a reduced $V_{DC}$ voltage of 1.5 kV. Such a slight difference in the $V_{DC}$ voltage results in a reduction in converter losses of

less than 10% (Figure 12A,B shows an experimental comparison), with the main qualitative behavior described above remaining valid.

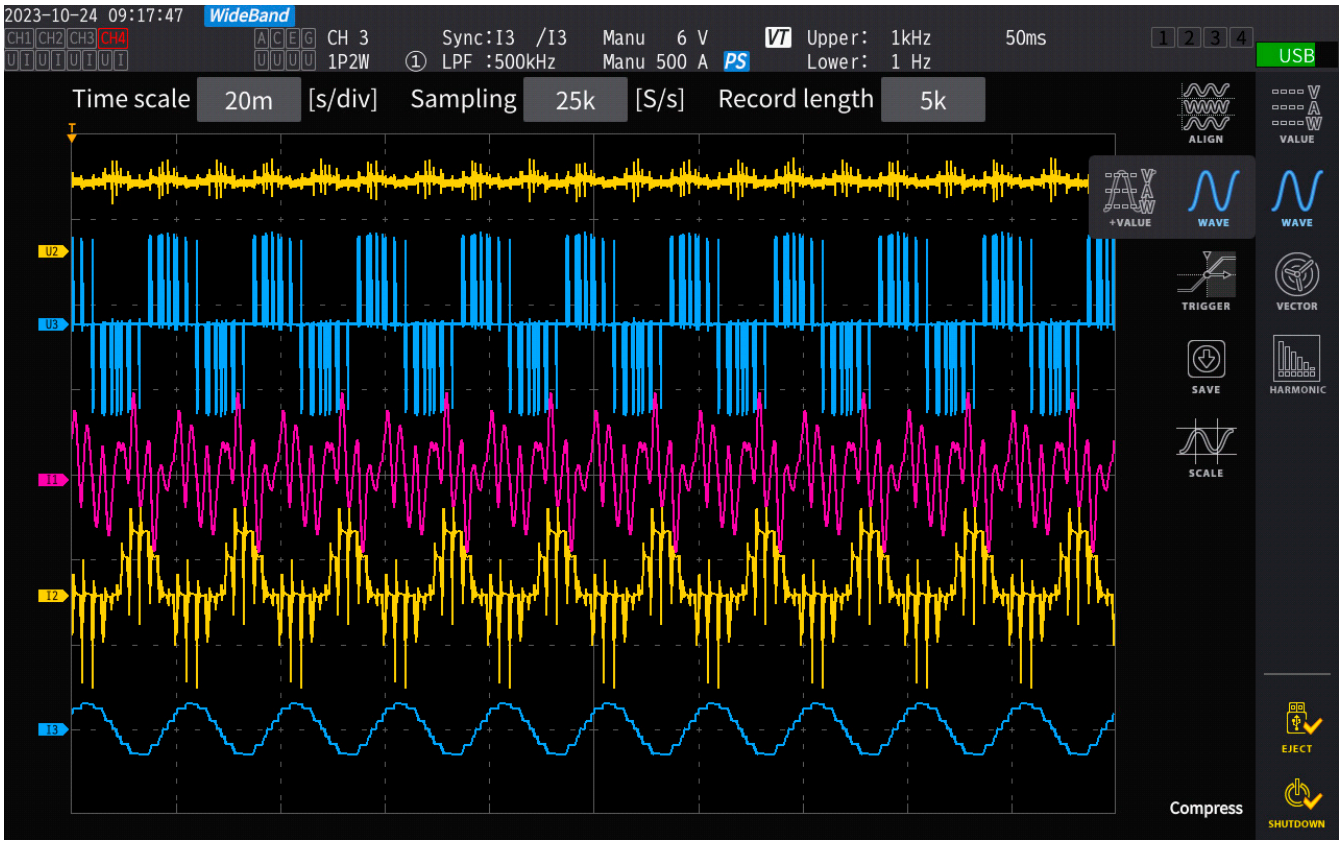
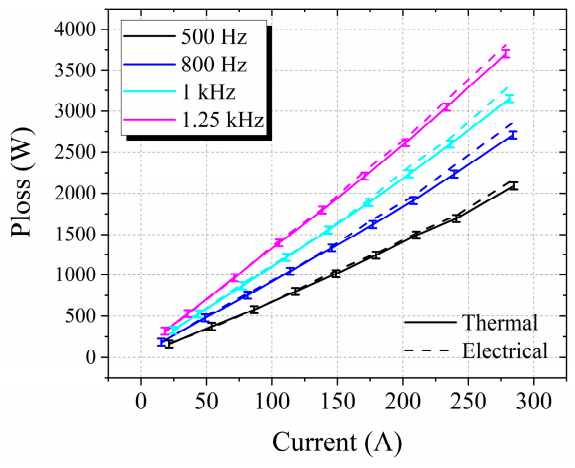
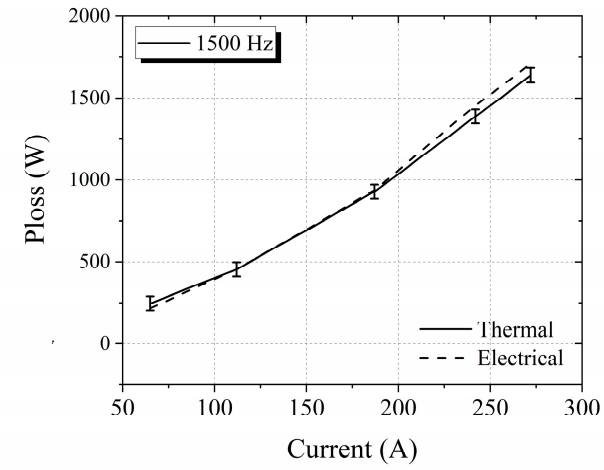



**Figure 7.** Back-to-back single-phase converter curves during steady state-run test. $V_{DC}$: 1.5 kV, $I_L$: 270 Arms, fs: 500 Hz, f: 50 Hz. Legends in the picture are: U2: DC link voltage ($V_{DC}$), U3: Inductor voltage ($V_L$), I1: Power supply current ($I_{in}$), I2: Circulated current ($I_{cir}$), and I3: Inductor current ($I_L$).

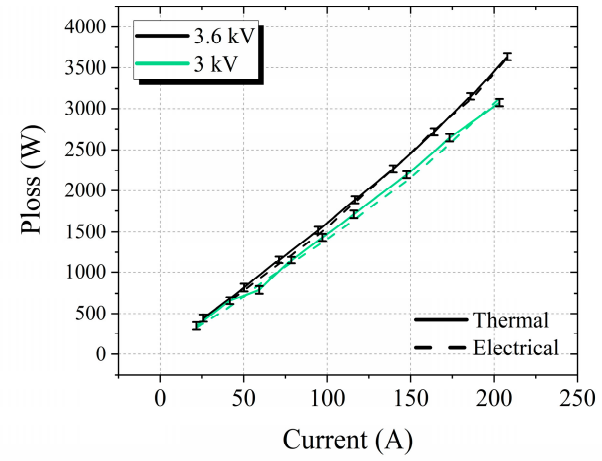



(**A**) 3.3 kV Si IGBT




(**B**) 3.3 kV SiC MOSFET

**Figure 8.** *Cont.*




(**C**) 6.5 kV Si IGBT

**Figure 8.** (**A**) Experimental semiconductor losses from the B2B 3.3 kV Si-based single-phase converter during steady state-run test for different currents. The test conditions are: $V_{DC}$: 1.8 kV, $I_L$: 0–300 $A_{rms}$, fs: 500, 800, 1000, 1250 Hz, f: 50 Hz, M: 0.9. (**B**) Experimental semiconductor losses from the B2B 3.3 kV SiC-based single-phase converter ($R_G$: 24 Ω) during steady state-run test for different currents. The test conditions are: $V_{DC}$: 1.5 kV, $I_L$: 0–300 $A_{rms}$, fs: 1500 Hz, f: 50 Hz, M: 0.9. (**C**) Experimental semiconductor losses from the B2B 6.5 kV Si-based single-phase converter during steady state-run test for different currents. The test conditions are: $V_{DC}$: 3 and 3.6 kV, $I_L$: 0–210 $A_{rms}$, fs: 500 Hz, f: 50 Hz, M: 0.9.

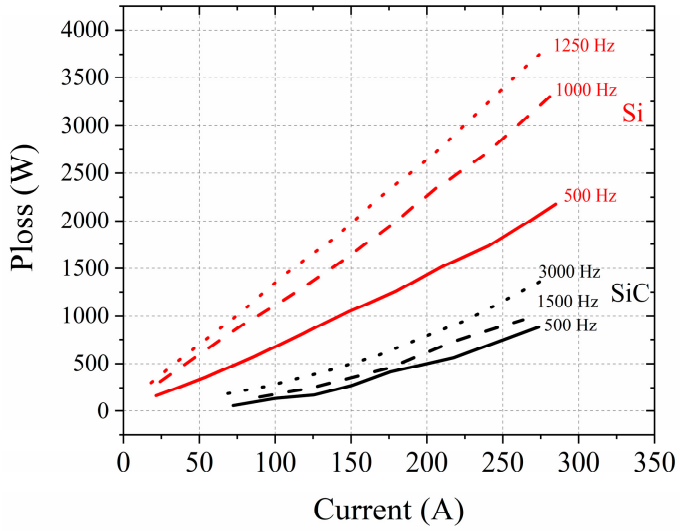
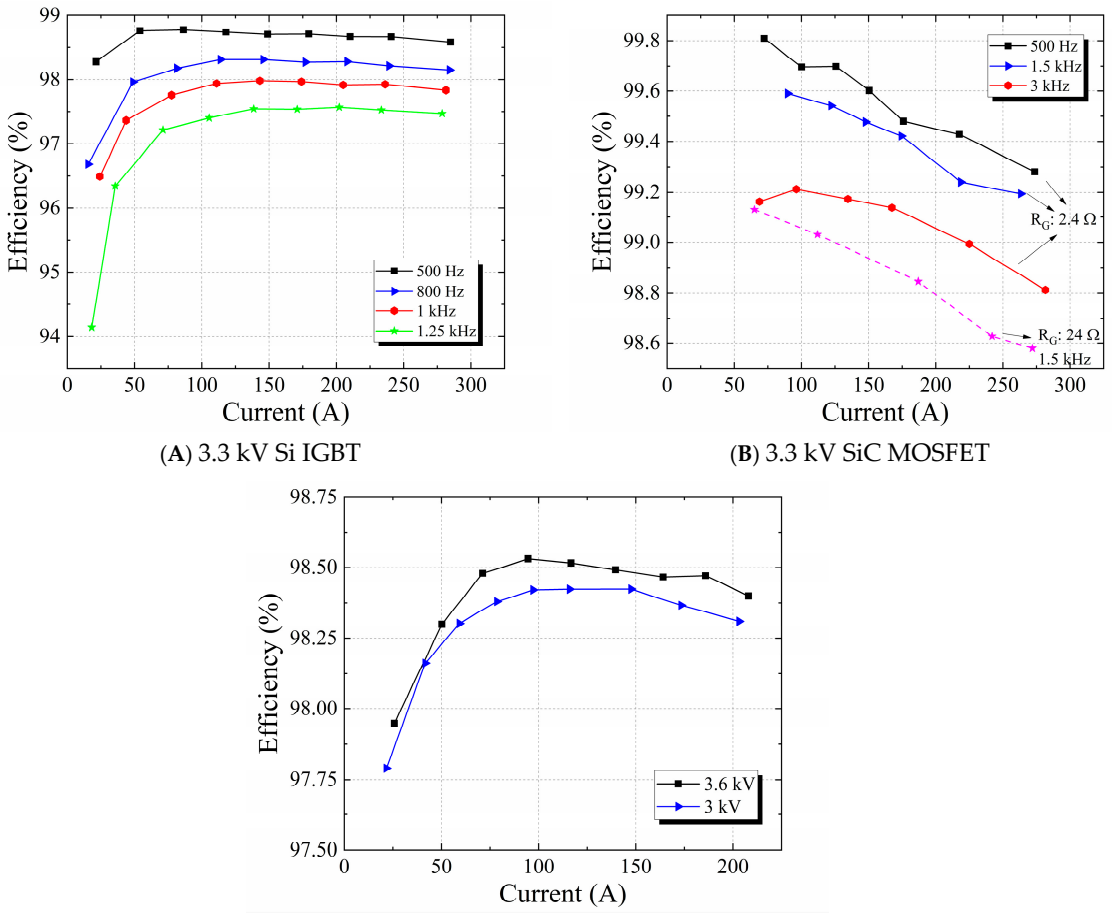



**Figure 9.** Semiconductor experimental converter losses (2 half-bridges) comparison between Si 3.3 kV silicon-based single-phase converter operating at $V_{DC}$: 1.8 kV, $I_L$: 0–300 $A_{rms}$, fs: 500, 800, 1000, 1250 Hz, f: 50 Hz, M: 0.9 and 3.3 kV SiC-based single-phase converter ($R_G$: 2.4 Ω) operating at $V_{DC}$: 1.5 kV, $I_L$: 0–300 $A_{rms}$, fs: 500, 1500, 3000 Hz, f: 50 Hz, M: 0.9.

Finally, the B2B converter efficiency using Equation (2) is evaluated and demonstrated in Figures 10A, 10B and 10C for the 3.3 kV Si IGBT, 3.3 kV SiC and 6.5 kV Si IGBT-based converters, respectively. In the case of the 3.3 kV Si IGBT-based converter, a peak efficiency of 98.7% is obtained for a 500 Hz switching frequency. With increasing switching frequency, the efficiency decreases, reaching values lower than 97.5% at 1250 Hz. Furthermore, a flat efficiency curve shape followed by a decay at around 50 $A_{rms}$, mainly related to the proportionally high conduction losses due to the knee shape in the forward device curve. Figure 10B shows the 3.3 kV SiC-based converter efficiency. The first characteristic observed

is the efficiency increase as the current decreases, similar to [11], reaching a peak of 99.8% at ~75 $A_{rms}$ for a 500 Hz switching frequency. This characteristic is expected due to the described unipolar behavior of SiC that presents excellent low on-state losses at partial-load conditions (due to the low junction temperature and linear curve behavior) together with low switching losses, outperforming Si IGBT by a large margin in this region (in a range of ~1 to ~1.5% efficiency improvement depending on the switching frequency). Thus, SiC is advantageous in mission profiles dominated by partial-load conditions. The efficiency reduction at higher current loads is also observed mainly due to the higher junction temperatures that degrade the on-state resistance, as described in Section 3.1. The switching frequency influence on the efficiency is less significant than for the case of the Si IGBT converter, as expected from the previous semiconductor loss analysis from Figure 9. An average efficiency reduction of around 0.5% by increasing the switching frequency from 500 up to 3 kHz is observed in the SiC case compared to an average efficiency reduction of around 1.2% by increasing the switching frequency from 500 up to only 1.25 kHz for the Si case. This characteristic shows the advantage of SiC devices in high-frequency power converters. Finally, the gate resistance increase promotes an almost constant efficiency reduction of about 0.5% through the investigated current range at a switching frequency of 1.5 kHz for the SiC converter.

The 6.5 kV Si IGBT-based converter behaves similarly to the 3.3 kV IGBT case, with an efficiency lower than 98.5% at a 3 kV DC link and 500 Hz switching frequency.




(**A**) 3.3 kV Si IGBT

(**B**) 3.3 kV SiC MOSFET

(**C**) 6.5 kV Si IGBT

**Figure 10.** (**A**) 3.3 kV Si IGBT-based experimental converter efficiency during steady state-run test for different currents. The test conditions are: $V_{DC}$: 1.8 kV, $I_L$: 0–300 $A_{rms}$, fs:

500, 800, 1000, 1250 Hz, f: 50 Hz, M: 0.9. (**B**) 3.3 kV SiC MOSFET-based experimental converter efficiency during steady state-run test for different currents. The test conditions are: $V_{DC}$: 1.5 kV, $I_L$: 0–300 $A_{rms}$, fs: 500, 1500, 3000 Hz, f: 50 Hz, M: 0.9; $R_G$: 2.4 Ω and $V_{DC}$: 1.5 kV, $I_L$: 0–300 $A_{rms}$, fs: 1500 Hz, f: 50 Hz, M: 0.9, $R_G$: 24 Ω. (**C**) 6.5 kV Si IGBT-based experimental converter efficiency during steady state-run test for different currents. The test conditions are: $V_{DC}$: 3 and 3.6 kV, $I_L$: 0–210 $A_{rms}$, fs: 500 Hz, f: 50 Hz, M: 0.9.

## 4. Electrothermal Power Converter Model

An electrothermal simulation model was developed to accurately perform system simulations and predict the performance of railway traction inverters. A state-of-the-art approach implements a behavioral model based on experimental forward and switching loss curves and the power modules' thermal impedance characteristics. The model structure was developed in PLECs. Every simulation step receives the device voltage, current, and junction temperature as input, which are calculated from the previous step based on the Kirchhoff's circuital laws and the thermal model. The received inputs and the power module's electrical parameters are then used to calculate the device's total losses (conduction + switching losses). The power module's electrical parameters (static and switching loss curves) are obtained from the experimental characterization or the device datasheet. Such parameters should be given at 25 and 125 °C to allow interpolation across the full operating temperature range. The calculated power losses are the input of the thermal model simulation block. This model is constructed from the association of thermal resistances and capacitances obtained from the device datasheets. The output of this thermal model generates the new junction temperatures that will be used in the next simulation step until the simulation reaches a steady state.

Figure 11 shows the thermal impedance model for the Si and SiC half-bridge power modules. The junction-to-case impedance (Zthj-c) is modeled with the datasheet Foster model. The device and cold plate datasheets provide the case-to-cold plate (considering 1 W/m.K grease) and cold plate to coolant thermal resistances (Rth), respectively. The used parameters are indicated in Table 2. The case-to-cold plate and cold plate to coolant thermal resistances are subjected to significant variation due to experimental mounting conditions and thermal paste conductivity and required a slight parameter tuning to match experimental results. It is important to emphasize here that in the selected thermal model, the thermal coupling between the devices happens at the cold plate modeled as an isothermal connection point. Furthermore, the SiC module presents only two devices since no antiparallel diode is present due to the power MOSFET's bidirectional property. The selected simplified thermal model provides good accuracy for estimating junction temperatures with low computational effort, as shown in the next paragraphs, not requiring complex modeling considerations.

**Table 2.** Implemented thermal resistance values in simulation.

| | **Si IGBT 3.3 kV/450 A** | **SiC MOSFET 3.3 kV/500 A** | **Si IGBT 6.5 kV/300 A** |
|---|---|---|---|
| Equivalent $Rth_{\text{junction to case}}$ | IGBT: 31 K/kW<br>Diode: 54 K/kW | 46.3 K/kW | IGBT: 33.4 K/kW<br>Diode: 52.4 K/kW |
| $Rth_{\text{case-coldplate}}$ | IGBT: 30 K/kW<br>Diode: 35 K/kW | 40 K/kW | IGBT: 23 K/kW<br>Diode: 40 K/kW |
| $Rth_{\text{coldplate-water}}$ | 15 K/kW | 10 K/kW | 15 K/kW |

In order to validate the proposed simulation model, each operation point from the B2B converter was simulated and compared to the experimental results. Figure 12 compares

simulation and experimental data in terms of power losses. The simulation followed the expected behavior for all tested cases with a maximum error of 200 W for the 3.3 kV Si IGBT-based converter case. For the SiC case, the maximum deviation was about 100 W, and for the 6.5 kV Si IGBT case, it was always smaller than 60 W. It is clear from the curves that the error is mainly systematic through the current range for most cases, with an exception for the 6.5 kV case where the match is close to optimal. Such systematic error may be related to the case-to-cold plate and cold plate to coolant thermal resistances that are subjected to significant uncertainty due to experimental mounting conditions and thermal paste conductivity as well as the simplified thermal model selection [28].

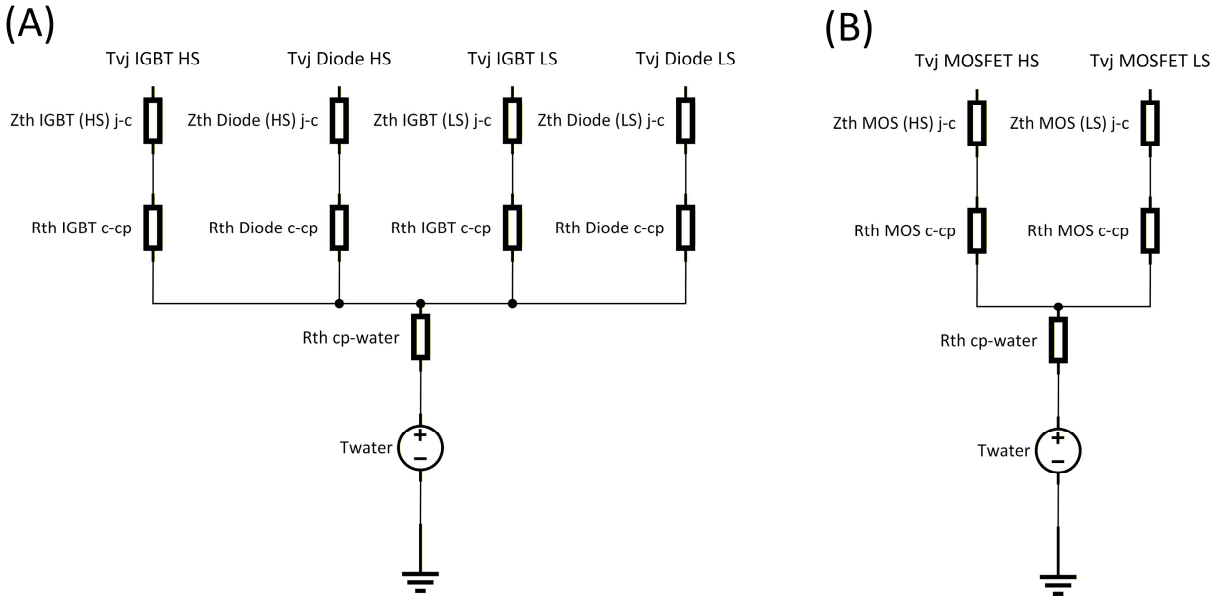



**Figure 11.** (**A**) Thermal impedance model of the Si IGBT half-bridge module on top of the cold plate. (**B**) Thermal impedance model of the SiC MOSFET half-bridge module on top of the cold plate. Abbreviations: Zth: thermal impedance, Rth: thermal resistance, HS: high side, LS: low side, j-c: junction to case, c-cp: case to cold plate, cp-water: cold plate to water, Tvj: junction temperature, Twater: water temperature.

The simulation always presents smaller values than the experimental values. Such systematic error provides a predictable simulation behavior for all cases, generating an average error when comparing Si and SiC technologies in the range of about 100 W. The accuracy achieved is excellent for comparison purposes between Si and SiC technologies as the expected power loss differences between both technologies (based on experimental data) are around 300 W at low current (50 $A_{rms}$) and more than 1000 W at high currents (with delta values close to 3000 W depending on the converter operation conditions). It is also essential to remember that the most critical region is at currents higher than 100 $A_{rms}$, where the converter operates most of the time, and higher losses are obtained. At regions close to 0 A, the losses are much smaller, and the accuracy (experimental or numerical) is naturally reduced due to the small values involved.

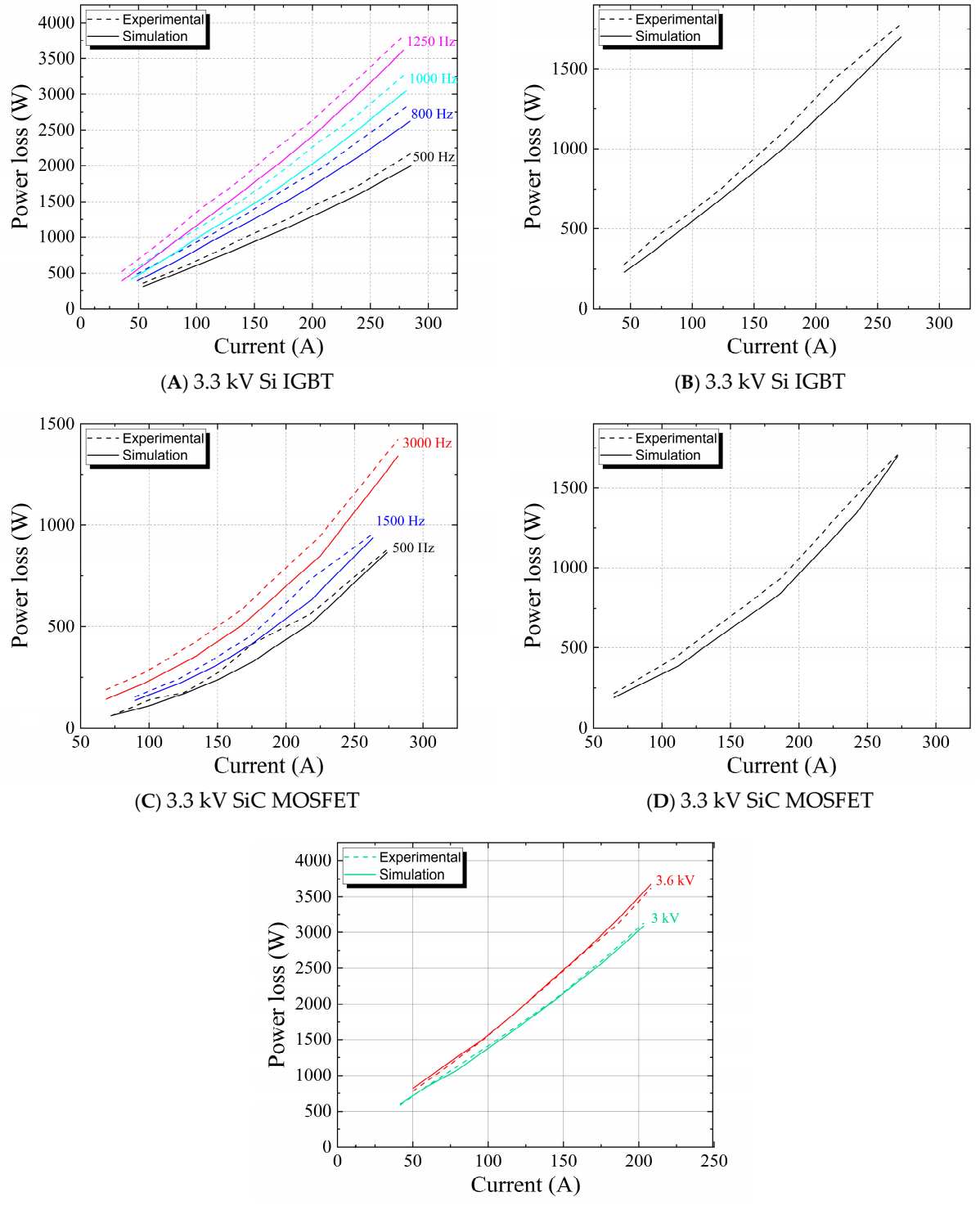



**Figure 12.** (**A**) 3.3 kV Si IGBT-based converter losses comparison between simulation and experimental data. The test conditions are: $V_{DC}$: 1.8 kV, $I_L$: 0–300 $A_{rms}$, fs: 500, 800, 1000, 1250 Hz, f: 50 Hz, M: 0.9. (**B**) 3.3 kV Si IGBT-based converter losses comparison between simulation and experimental data. The test conditions are: $V_{DC}$: 1.5 kV, $I_L$: 0–300 $A_{rms}$, fs: 500 Hz, f: 50 Hz, M: 0.9. (**C**) 3.3 kV SiC MOSFET-based converter ($R_G$: 2.4 Ω) losses comparison between simulation and experimental data. The test conditions are: $V_{DC}$: 1.5 kV, $I_L$: 0–300 $A_{rms}$, fs: 500, 1500, 3000 Hz, f: 50 Hz, M: 0.9. (**D**) 3.3 kV SiC MOSFET-based converter ($R_G$: 24 Ω) losses comparison between simulation and experimental data. The test conditions are: $V_{DC}$: 1.5 kV, $I_L$: 0–300 $A_{rms}$, fs: 1500 Hz, f: 50 Hz, M: 0.9. (**E**) 6.5 kV Si IGBT-based converter losses comparison between simulation and experimental data. The test conditions are: $V_{DC}$: 3 and 3.6 kV, $I_L$: 0–210 $A_{rms}$, fs: 500 Hz, f: 50 Hz, M: 0.9.

## 5. Railway Traction Systems

### *5.1. Commercial Topologies and Configurations*

The typical rail voltages can vary from 750 Vdc to 25 kVac [29,30]. In general, higher voltages are converted to achieve DC link voltages of 750 V up to 3 kV for the traction inverter. There are also cases of DC catenaries at 3 kV, not requiring transformers or rectifier circuits. When the rectification is required, it can have a unidirectional or bidirectional front-end topology depending on whether regenerative energy is desired to flow back to the catenary system. Additional DC-DC converters may be implemented to add functionalities, such as onboard batteries for operation in non-electrified routes. In this work, we focused on traction inverters used in metros, trains and locomotives with a typical DC link voltage of 1500 V or 3000 V, which are common in practice. The industry standard choice for a 1.5 kV DC link voltage is a three-phase, two-level (2L) inverter topology with 3.3 kV power switches [29]. In the case of the 3 kV DC link, the same topology is used with 6.5 kV switches, and it is also an option to implement three-level (3L) topologies like the traditional active neutral-point-clamped (ANPC) topology [31,32] with 3.3 kV switches (Figure 13). The nominal power of these inverters is in the range of 150 kW–1.4 MW [29].

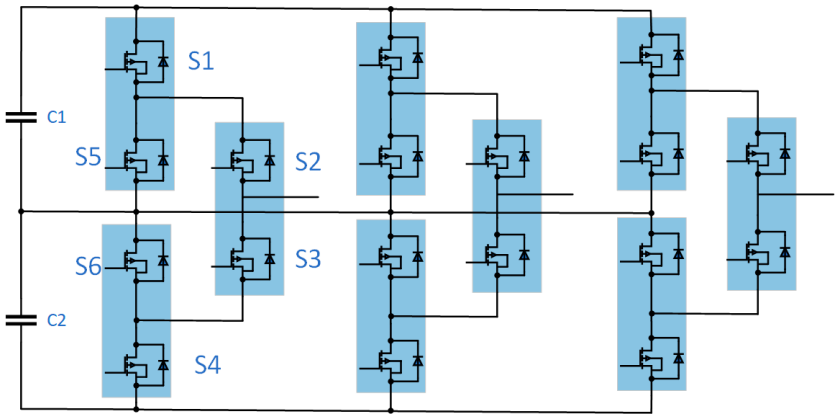



**Figure 13.** ANPC topology, with the positioning of the half-bridge power modules indicated inside the blue boxes. These boxes also indicate the positioning of the cold plates and thermal coupling between switches. Switch names are shown only for one phase.

From a system perspective, the topology choice is typically driven by a combination of: device voltage margin and current rating so that the circuits can safely operate within a safety operating area (SOA); target efficiency across partial-load regions that dominate real operation; loadability under thermal constraints; and insulation/EMC constraints driven by cable length and $dv/dt$. Two-level VSC solutions are attractive for simplicity and robustness, whereas three-level ANPC solutions can reduce voltage steps and improve harmonic performance, potentially relaxing motor-side constraints. In this work, these trade-offs are quantified consistently using experimentally validated electrothermal models under representative railway operating conditions.

Regarding the positioning of each power module in the two-level VSC topology, a LinPak module is composed of one power switch on the high side and one on the low side (half-bridge module), leading to one module per phase. For the three-level topology case, the positioning of the LinPak modules is indicated in the blue boxes in Figure 13.

For the 1.5 kV DC link voltage, two-level VSC topologies based on 3.3 kV Si and SiC LinPak power modules have been compared. In the case of 3 kV DC link railway systems, a two-level topology with 6.5 kV Si IGBT LinPak power modules is compared to a three-level ANPC topology built with 3.3 kV SiC power modules. The comparisons are always performed within the configurations from the same DC link voltage

class. Tables 3 and 4 show the simulated topology configurations and the devices used for the 1.5 kV and 3 kV DC link traction systems, respectively. All devices have been characterized and had their electrothermal models validated in previous chapters of this paper (see Sections 3 and 4). The 2.4 and 24 Ω gate resistance cases were investigated to compare the performance of railway inverters operating with high (~38 V/ns) and low speed switching (~7 V/ns). Such cases may influence the requirement of an additional *dv*/*dt* filter to protect the motor insulation. For the 3 kV DC link case, the 3.3 kV switches had their parameters downrated to 300 A to match the 6.5 kV Si IGBT current rating. As a result, a fair comparison between same current rating devices can be performed.

**Table 3.** Simulated topology configurations for the 1.5 kV DC link traction system.

| Topology | Device | Gate Resistance (Ω) | Switching Frequency (Hz) |
|---|---|---|---|
| 2-Level | Si IGBT 3.3 kV/450 A | 1.5 | 500 |
| 2-Level | SiC MOSFET 3.3 kV/500 A | 2.4 | 500 |
| 2-Level | SiC MOSFET 3.3 kV/500 A | 24 | 500 |
| 2-Level | SiC MOSFET 3.3 kV/500 A | 2.4 | 1500 |
| 2-Level | SiC MOSFET 3.3 kV/500 A | 24 | 1500 |

**Table 4.** Simulated topology configurations for the 3 kV DC link traction system.

| Topology | Device | Gate Resistance (Ω) | Switching Frequency (Hz) |
|---|---|---|---|
| 2-Level | Si IGBT 6.5 kV/300 A | 7.5 | 500 |
| 3-Level ANPC | SiC MOSFET 3.3 kV/300 A | 2.4 * | 500 |
| 3-Level ANPC | SiC MOSFET 3.3 kV/300 A | 24 * | 500 |
| 3-Level ANPC | SiC MOSFET 3.3 kV/300 A | 2.4 * | 1500 |
| 3-Level ANPC | SiC MOSFET 3.3 kV/300 A | 24 * | 1500 |

* The indicated gate resistance is from the characterized power module (3.3 kV/500 A SiC MOSFET) that had the current downrated for the 3L topology simulation.

The devices' downrating is based on [33,34], where the thermal resistance, and on-state resistance are linearly scaled according to Equations (3) and (4). For the SiC dynamic performance, the switching losses are small and the variation in the switching losses versus die size is negligible as demonstrated by [35], with a change of about 37% of the switching losses when the device current rating changed by 350% [35]. Thus, the same switching loss values from the 500 A module were assumed for the 300 A module.

$$R_{DSon,rated} = R_{DSon,nom} \times I_{nom}/I_{rated} \quad (3)$$

$$R_{thjc,rated} = R_{thjc,nom} \times I_{nom}/I_{rated} \quad (4)$$

Regarding the modulation techniques implemented in commercial traction inverters, several modulation strategies may be used, such as Sinusoidal PWM (SPWM), Space vector modulation (SVM), and Selective harmonic elimination [29]. This work implemented the Sinusoidal PWM (SPWM) for the two-level VSC topology. In the case of the three-level ANPC converter, several other variations based on the described options can be performed due to the redundant states that can be used to balance the power loss between the switches [31]. More advanced techniques implement online junction temperature estimation to choose real-time transitions [36]. Here, a simple SPWM technique with the commutations cells formed by S1, S3, S5 and S2, S4, and S6 (see Figure 13) alternating between line and switching frequency during negative and positive half cycles and a

single neutral state in order to reduce conduction losses in devices S2, S3, S5 and S6. Such an option is described in [32,36], presenting good results for SiC devices and an easy implementation with similar signal generation to an NPC topology [32].

### *5.2. Railway Inverters Efficiency*

This section evaluates the efficiency of 1.5 and 3 kV DC link-based traction inverters (two-level and three-level ANPC topologies). The load current was an ideal sine-wave current source. The simulation parameters are shown in Table 5. The load power factor (PF) was modeled based on a typical MV motor power factor profile [35]. The full load case (100%) was set for each converter configuration when the average junction temperature reached the maximum value of 125 °C. The selected switching frequencies were based on the following considerations:

**Table 5.** Inverter efficiency simulation parameters.

| | |
|---|---|
| DC link voltage | 1.5/3 kV |
| Modulation factor | 0.9 |
| Switching frequency | 500/1500 Hz |
| Fundamental frequency | 50 Hz |
| Load PF | Typ MV motor [35] |
| Water temperature | 40 °C |

500 Hz: Typical switching frequency of commercial Si IGBT-based railway traction inverter.

1500 Hz: With the implementation of SiC devices, due to the high-efficiency operation at higher switching frequencies, an increase in the switching frequency brings advantages to motor efficiency by reducing motor harmonic losses [37]. Additionally, higher frequency operation can reduce the motor noise [12]. The optimum switching frequency determination requires a combined characterization approach of the inverter with the motor [37]. Based on previous railway traction works with 3.3 kV SiC devices [11,12], an optimum switching frequency may be in the range of 800–2000 Hz. Based on these considerations, a switching frequency of 1500 Hz was selected.

The use of an ideal sine-wave current load is a traditional method for benchmarking inverter efficiency [25,38], not requiring deep analysis of the load (e.g., inclusion of motor models). However, it is well known that current harmonics may cause additional losses due to the presence of additional frequencies.

#### 5.2.1. 1.5 kV DC Link System

Figure 14 shows the simulated efficiencies for the 1.5 kV DC link railway inverters. The behavior is similar to Figure 10, with the physical explanation of the observed shape detailed in Section 3.3. Here, the focus is on the numerical efficiency values of the different topology configurations. The Si IGBT topology presents the lowest efficiency value with a flat behavior of around 99.2% above 100 A. The SiC configurations at 500 Hz and 1500 Hz with low gate resistance and at 500 Hz with high gate resistance present a considerable efficiency gain compared to the Si configuration with similar efficiency values. The SiC configuration at 1500 Hz and high gate resistance presents a higher efficiency degradation due to the higher frequency and switching losses. Overall, the SiC topologies with low gate resistances at 500 and 1500 Hz and the one with high gate resistance at 500 Hz are promising candidates for efficiency optimization compared to the Si IGBT inverter.

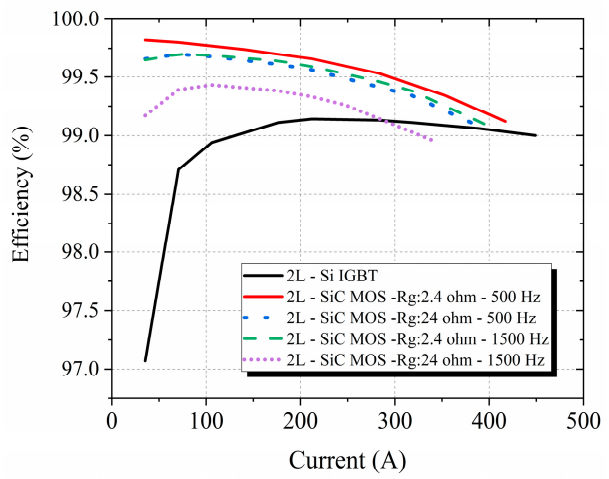



**Figure 14.** Simulated efficiency curves for 1.5 kV DC link railway inverters.

#### 5.2.2. 3 kV DC Link System

Figure 15 shows similar behavior to Figure 14, with the main difference that the SiC efficiency curves do not cross the two-level Si IGBT efficiency curve, displaying a flatter behavior. Overall, the SiC topologies are promising for efficiency optimization compared to the 6.5 kV Si IGBT-based inverter.

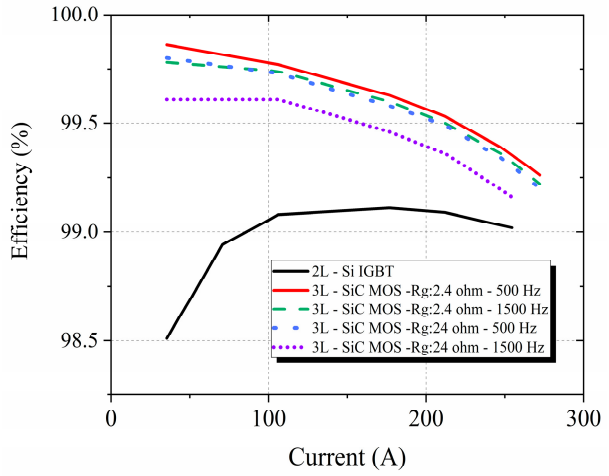



**Figure 15.** Simulated efficiency curves for 3 kV DC link railway inverters.

### *5.3. Railway Inverters Loadability*

The loadability analysis evaluates the maximum output power a converter can provide for a certain switching frequency. This assessment is essential to compare the maximum power rating of distinct converter designs and provide essential information to evaluate the converter costs per kWh.

In this section, the simulations were performed considering a maximum average junction temperature of 125 °C, typical of MV power modules. The parameters are similar to those from the previous section with the following differences:

- Modulation factor of 1 for the two- and three-level topologies.
- Power factor of 1.

The above conditions may represent a worst-case scenario for the three-level ANPC topology and were also considered for the two-level case.

#### 5.3.1. 1.5 kV DC Link System

The loadability analysis from Figure 16 shows that the SiC at low gate resistances can operate up to 5000 Hz, not aggressively deteriorating the converter power rating. A reduction in the maximum current of about 15% is observed when operating at 5000 Hz and only about 5% reduction when operating at 1500 Hz. This characteristic is advantageous for designs where high switching frequency operation can considerably improve power converter density, like grid-tied converters with bulky output sine filters [24]. Additionally, the analysis shows that an increase from 500 to 1500 Hz for railway applications slightly penalizes the converter power rating. In the SiC option with high gate resistance, a reduction of around 40% when operating at 5000 Hz and around 12% when operating at 1500 Hz is assessed. The Si IGBT presents a very high degradation of the converter rating with switching frequencies higher than 500 Hz due to the high Si IGBT switching losses. A reduction of about 36% is observed with an operation of only 1500 Hz. This limitation factor is why these converters operate at low switching frequencies to not aggressively increase the cost per kWh. Interestingly, at 500 Hz, the Si IGBT presents a slightly better current capability than the SiC at low gate resistance, presenting a power extension of around 10% over the SiC (low gate resistance) topology. This characteristic comes from the higher on-state losses of the SiC device at high currents and high temperatures, as demonstrated in Section 3.1.

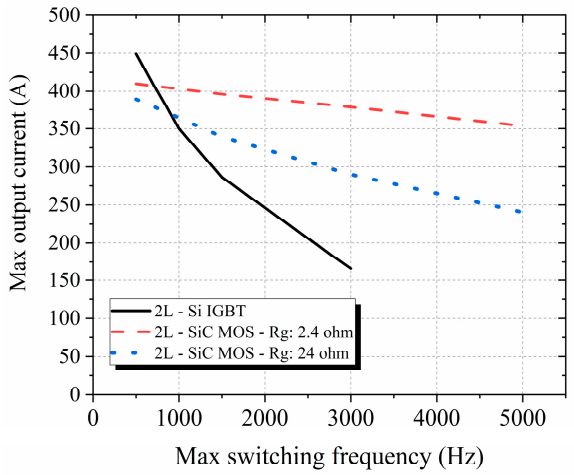



**Figure 16.** Simulated loadability curves for 1.5 kV DC link railway inverters.

#### 5.3.2. 3 kV DC Link System

Figure 17 shows the three-level SiC topology at low gate resistance with an almost constant current output capability in the switching frequency range up to 3000 Hz. The same topology with a higher gate resistance shows the current reduction with the increased switching frequency. A current reduction of about 15% from the 500 Hz operation point is observed at the frequency of 1500 Hz. At 500 Hz, it presents the same current capability as the three-level SiC topology with low gate resistance. Finally, the two-level Si IGBT topology presents a very high degradation of the converter rating for frequencies higher than 500 Hz, reaching a current reduction of about 55% at 1500 Hz compared to 500 Hz. This fact justifies testing and inverter design for these power modules only up to around 500 Hz, since higher switching frequencies require aggressive derating of the nominal inverter current. In a nutshell, the three-level SiC topology with low gate resistance can have an operation point up to 3 kHz, maintaining the converter rating. Such characteristic is good for improving motor losses due to better voltage harmonic content while keeping the converter cost per kWh. A switching frequency of 1500 Hz may be the best choice since the efficiency is still high, as shown in Figure 15, not negatively affecting the heatsink

volume required, energy loss costs and carbon footprint. The three-level topology with high gate resistance operating at 500 Hz presents the same current capability as the three-level topology with low gate resistance at 1500 Hz. The efficiency curve behavior is also quite similar between both combinations. A possible advantage of the three-level SiC topology with high gate resistance could be to avoid using an output $dv/dt$ filter depending on the motor connections. The lower voltage harmonic quality due to the lower switching frequency may be a disadvantage, which may increase motor losses.

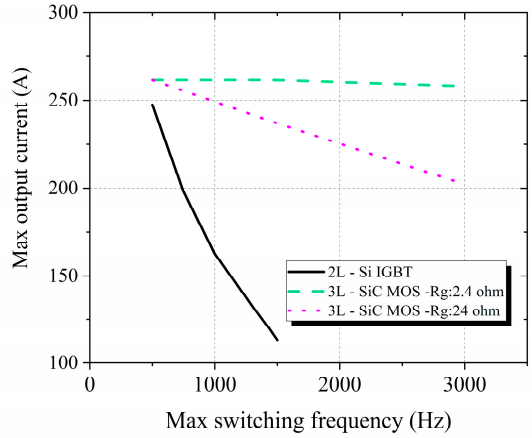



**Figure 17.** Simulated loadability curves for 3 kV DC link railway inverters.

### *5.4. Life Cycle Energy Assessment of Traction Inverters*

#### 5.4.1. Power Loss Investigation in a Drive Cycle

In order to make a performance assessment in a realistic operation environment, the energy loss evaluation of the proposed topologies was performed under a realistic drive cycle [6] and shown here in Figure 18. The validated semiconductor electrothermal parameters were used in the simulation. This drive-cycle evaluation directly links the partial-load conduction advantage observed in Section 3.1 to mission-level energy savings, because a substantial fraction of operating time occurs below nominal current. Based on what was learned in the previous sections regarding efficiency and loadability, the analyzed topology configurations are shown in Tables 6 and 7. From all initially proposed topologies in Tables 3 and 4, we discarded the two-level 3.3 kV SiC configuration with low gate resistance at 500 Hz due to the similar efficiency and current capability compared to the 1500 Hz configuration that can bring further advantages through reduced motor losses. The two-level 3.3 kV SiC at high gate resistance and 1500 Hz switching frequency was also discarded due to the significant efficiency and loading capability deterioration observed at this switching frequency.

**Table 6.** 1.5 kV DC link railway inverter simulated configurations.

| Topology | Switch. Frequency (Hz) | Twater (°C) | Multiplicator (K) |
|---|---|---|---|
| 3.3 kV Si/$R_G$: 1.5 Ω 2-level | 500 | 40 | 1 |
| | 500 | 40 | 50 |
| | 500 | 70 | 1 |
| | 500 | 70 | 50 |
| 3.3 kV SiC/$R_G$: 24 Ω 2-level | 500 | 40 | 1 |
| | 500 | 40 | 50 |
| 3.3 kV SiC/$R_G$: 2.4 Ω 2-level | 1500 | 40 | 1 |
| | 1500 | 40 | 50 |
| | 1500 | 70 | 1 |
| | 1500 | 70 | 50 |

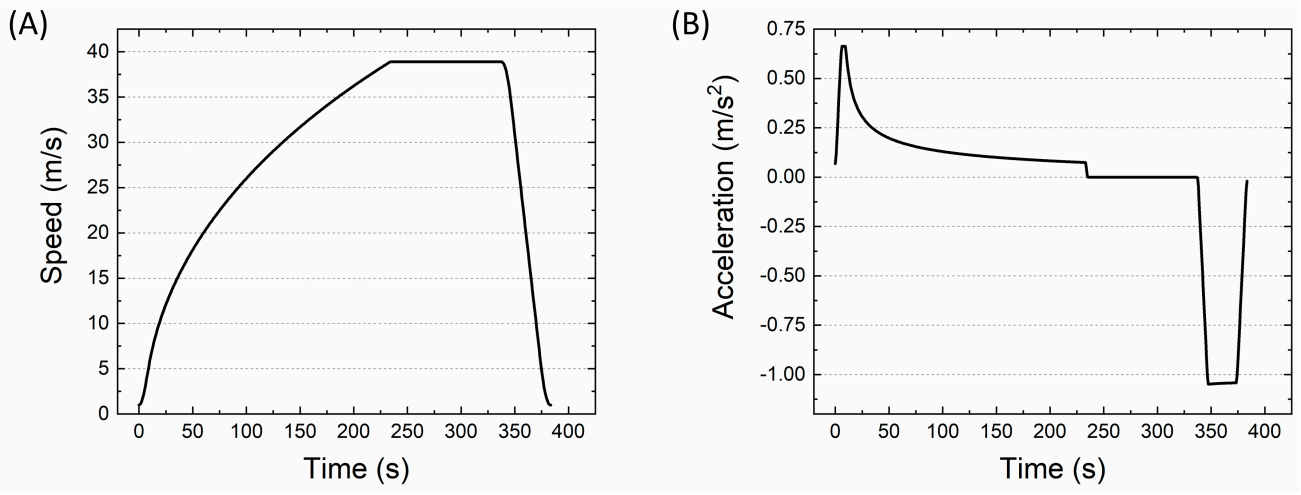



**Figure 18.** Drive cycle (**A**) and acceleration profile (**B**) from a typical train route. These profiles are used as input for the railway traction inverter simulations [6].

**Table 7.** 3 kV DC link railway inverter simulated configurations.

| Topology | Switch. Frequency (Hz) | Twater (°C) | Multiplicator (K) |
|---|---|---|---|
| 6.5 kV Si/$R_G$: 7.5 Ω 2-level | 500 | 40 | 1 |
| | 500 | 40 | 55 |
| | 500 | 70 | 1 |
| | 500 | 70 | 55 |
| 3.3 kV SiC/$R_G$: 24 Ω 3-level ANPC | 500 | 40 | 1 |
| | 500 | 40 | 55 |
| 3.3 kV SiC/$R_G$: 2.4 Ω 3-level ANPC | 1500 | 40 | 1 |
| | 1500 | 40 | 55 |
| | 1500 | 70 | 1 |
| | 1500 | 70 | 55 |

For the 3 kV DC link railway systems, the same strategy was applied, discarding the 3.3 kV three-level at low gate resistance and 500 Hz as well as the 3.3 kV three-level at high gate resistance and 1500 Hz (Table 4). MV induction motors formed the load. In the case of the 1.5 kV DC link railway systems, four medium-voltage induction motors compose the load. This is a typical situation in trains where up to four motors can be connected to the same inverter output [29]. The power converters analyzed have a nominal power rating of around 600–900 kW, considering the thermal criteria used in Section 5.3. The four motors have a nominal power of 640 kW (each 160 kW) and a nominal voltage of 1287 V. This value is within the range of a typically adopted motor voltage for converters with a DC link of 1500–1800 V [6,29]. Reference [39] details the electrical parameters of the motor used in the simulation. For the 3 kV DC link railway systems, the same motor parameters were slightly adapted to reach a nominal power of 560 kW, and a nominal voltage of 2400 V, a typical voltage rating used in railway systems at 3 kV DC link [29]. For this case, since the motor power rating is 560 kW and the converters have power ratings in the range of 700–900 kW, two motors were chosen as the load.

Further details of the train model and control strategy for the proposed load cycle are described in [6]. In this manuscript, the drive cycle was investigated under distinct operational conditions to evaluate the Si and SiC semiconductors at distinct junction temperatures and currents. Two distinct water temperatures (40 and 70 °C) were considered to investigate inverter efficiency with an offset in semiconductor junction temperatures during the drive cycle. In addition, we have artificially included a multiplication factor (K) in the squared speed term from Equation (5), which represents the drag force (Fd) the train

is subjected to during the drive cycle in relation to train speed (v) and weight (G) [6]. In general, the cruising region has the lowest current, while acceleration and braking have the highest currents due to high inertial acceleration. Such a multiplication factor to increase the dragging force during cruising could represent a situation where the train operates at high-speed uphill, requiring more traction power from the inverter.

$$Fd = \left(0.75 + 0.0011664 * K * v^2\right) * G \quad (5)$$

5.4.1.1. 1.5 kV DC Link System

The topology configurations from Table 6 were simulated, and the results are indicated in Table 8. Figure 19 shows the device temperature for three different drive cycle conditions when the water temperature and the multiplicator value are changed. Figure 19A shows the case when K = 1 and the water temperature equals 40 °C. The highest temperature is achieved during the train braking, reaching the highest current. During the cruise phase, the temperature is the lowest since the opposing force is not significant. In Figure 19B, increasing K increases the device current during cruising and the device temperature reaches its peak during that phase. Finally, Figure 19C shows the case when the water temperature is increased to 70 °C. Since K = 1 as in the first case (Figure 19A), the temperature profile shape is similar to Figure 19A with an additional offset in the temperature values.

**Table 8.** 1.5 kV DC link railway inverters simulated configurations. The drive cycle energy loss per phase is demonstrated for each configuration. Additionally, the saved energy per phase in comparison to the equivalent Si-based topology (same Twater and Multiplicator) is shown in absolute values and percentage.

| Topology Configuration | Switching Frequency (Hz) | Twat (°C) | Multiplicator (K) | $E_{loss}$/Phase (kWh) | Saved Energy-Compared to Si (kWh) | Saved Energy-Si Case as Reference (%) |
|---|---|---|---|---|---|---|
| 3.3 kV Si $R_G$: 1.5 Ω | 500 | 40 | 1 | 0.04853 | - | - |
| 3.3 kV Si $R_G$: 1.5 Ω | 500 | 40 | 50 | 0.08550 | - | - |
| 3.3 kV Si $R_G$: 1.5 Ω | 500 | 70 | 1 | 0.05197 | - | - |
| 3.3 kV Si $R_G$: 1.5 Ω | 500 | 70 | 50 | 0.09192 | - | - |
| 3.3 kV SiC $R_G$: 2.4 Ω | 1500 | 40 | 1 | 0.01772 | 0.03081 | 63.5 |
| 3.3 kV SiC $R_G$: 2.4 Ω | 1500 | 40 | 50 | 0.04827 | 0.03723 | 43.5 |
| 3.3 kV SiC $R_G$: 2.4 Ω | 1500 | 70 | 1 | 0.02128 | 0.03069 | 59 |
| 3.3 kV SiC $R_G$: 2.4 Ω | 1500 | 70 | 50 | 0.05856 | 0.03336 | 36.3 |
| 3.3 kV SiC $R_G$: 24 Ω | 500 | 40 | 1 | 0.02169 | 0.02684 | 55.3 |
| 3.3 kV SiC $R_G$: 24 Ω | 500 | 40 | 50 | 0.05757 | 0.02793 | 32.6 |

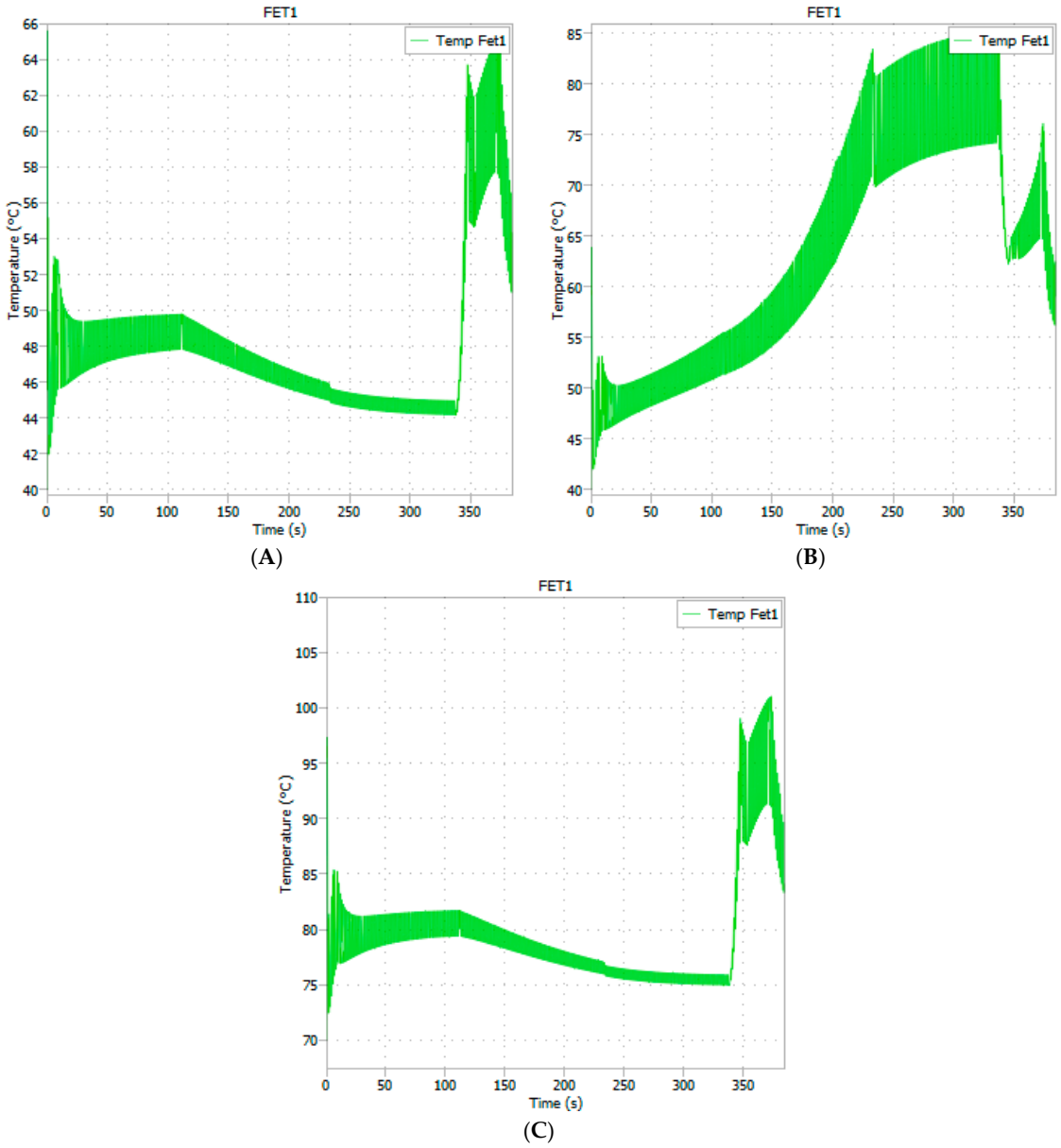



**Figure 19.** (**A**) MOSFET temperature during drive cycle at Twater: 40 °C, multiplicator (K): 1, fs: 1500 Hz, $R_G$: 2.4 Ω. (**B**) MOSFET temperature during drive cycle at Twater: 40 °C, multiplicator (K): 50, fs: 1500 Hz, $R_G$: 2.4 Ω. (**C**) MOSFET temperature during drive cycle at Twater: 70 °C, multiplicator (K): 1, fs: 1500 Hz, $R_G$: 2.4 Ω.

Table 8 shows that the most significant energy savings per phase occur during partial-load conditions and lower temperatures, reaching potential energy savings of up to 63% of the losses from the Si IGBT case for the low gate resistance configuration. Even with the water temperature being increased up to 70 °C, the energy savings are still 59%. A significant energy savings reduction occurs when the current increases during the cruising phase (increased K). The energy savings percentage is reduced to around 40% in that case.

5.4.1.2. 3 kV DC Link System

Table 9 shows the simulation results for the 3 kV DC link-based inverters. The same behavior as in the 1.5 kV DC link analysis is observed here, with the most significant factor reducing the energy loss savings being the current increase during the cruising phase (higher multiplication factor) followed by the temperature increase. The main difference is that the energy savings can reach around 60 to 74% for the low gate resistance case. This

was expected based on the efficiency curves from Section 5.2, where the efficiency at higher currents is better for the three-level topologies than the two-level topologies compared to the 1.5 kV DC link case. Consequently, the percentage energy loss savings per phase are higher.

**Table 9.** 3 kV DC link railway inverters simulated configurations. The drive cycle energy loss per phase is demonstrated for each configuration. Additionally, the saved energy per phase in comparison to the equivalent Si-based topology (same Twater and Multiplicator) is shown in absolute values and percentage.

| Topology Configuration | Switching Frequency (Hz) | Twat (°C) | Multiplicator (K) | $E_{loss}$/Phase (kWh) | Saved Energy-Compared to Si (kWh) | Saved Energy-Si Case as Reference (%) |
|---|---|---|---|---|---|---|
| 6.5 kV Si $R_G$: 7.5 Ω | 500 | 40 | 1 | 0.099463 | - | - |
| 6.5 kV Si $R_G$: 7.5 Ω | 500 | 40 | 55 | 0.13964 | - | - |
| 6.5 kV Si $R_G$: 7.5 Ω | 500 | 70 | 1 | 0.10706 | - | - |
| 6.5 kV Si $R_G$: 7.5 Ω | 500 | 70 | 55 | 0.15256 | - | - |
| 3.3 kV SiC ANPC $R_G$: 2.4 Ω | 1500 | 40 | 1 | 0.025394 | 0.07407 | 74.5 |
| 3.3 kV SiC ANPC $R_G$: 2.4 Ω | 1500 | 40 | 55 | 0.050183 | 0.08946 | 64 |
| 3.3 kV SiC ANPC $R_G$: 2.4 Ω | 1500 | 70 | 1 | 0.03111 | 0.07595 | 70.9 |
| 3.3 kV SiC ANPC $R_G$: 2.4 Ω | 1500 | 70 | 55 | 0.06169 | 0.09087 | 59.5 |
| 3.3 kV SiC ANPC $R_G$: 24 Ω | 500 | 40 | 1 | 0.03334 | 0.06606 | 66.4 |
| 3.3 kV SiC ANPC $R_G$: 24 Ω | 500 | 40 | 55 | 0.059296 | 0.08034 | 57.5 |

### *5.5. Lifetime Energy and $CO_2$-eq Savings*

The SiC inverter lifetime energy savings compared to the respective Si inverter will be detailed for one topology configuration (3.3 kV SiC, $R_G$: 2.4 Ω, two-level VSC). The same procedure is applied for the other cases, and the results are indicated in Tables 10 and 11 for the 1.5 kV DC link and the 3 kV DC link railway systems, respectively. Since different drive cycle conditions may occur, we considered the average saved energy across the distinct drive cycle conditions from Sections 5.4.1.1 and 5.4.1.2 for each topology configuration. The average saved energy per phase over one drive cycle for the two-level 3.3 kV SiC ($R_G$: 2.4 Ω) configuration compared to the Si IGBT topology is 0.033 kWh. The assumption of a train operation of 12 h per day leads to 108 drive cycle repetitions per day (drive cycle duration approximated to 400 s). Furthermore, it was assumed an annual train operation of 300 days, leading to an annual saved energy per phase of 1.069 MWh. In a 25-year lifetime and considering the whole inverter (three phases), the lifetime energy savings per inverter is 80.2 MWh by substituting the Si IGBT inverter with the SiC ($R_G$: 2.4 ohm)

inverter. From [6], it is well known that the use-phase is the dominant stage in terms of consumed energy, with the semiconductor manufacturing stage presenting a negligible contribution to the entire power converter life cycle (<0.3%). In this section, only the use-phase energy is considered in the inverter lifetime energy savings. The highest achieved lifetime savings was 200.7 MWh for the three-level SiC topology at low gate resistance. Such energy savings contribute to reduce the carbon footprint of the existing railway technology, helping to mitigate the effects of carbon dioxide emissions. This estimate was based on the potential energy savings and the carbon intensity generation in Germany in 2023 (381 $gCO_2$-eq/kWh). Values up to ~76 t $CO_2$-eq per inverter lifetime could be reduced by implementing SiC-based topologies. These values can be increased even more in countries where the carbon intensity generation is higher or by a more intensive use of the inverter during its lifetime.

**Table 10.** 1.5 kV DC link 3-phase inverter details and inverter lifetime energy and $CO_2$-eq savings (25 years) in relation to the 3.3 kV Si IGBT-based inverter.

| Inverter Configuration | Si—2 Level | SiC—2 Level $R_G$: 2.4 Ω | SiC—2 Level $R_G$: 24 Ω |
|---|---|---|---|
| Converter rating [kW] | 714 | 630 | 619 |
| Switching frequency [Hz] | 500 | 1500 | 500 |
| Lifetime energy savings compared to the Si inverter [MWh] | - | 80.2 | 66.5 |
| $CO_2$-eq saved [tons] * | - | 30.6 | 25.3 |

* Carbon intensity generation of 381 $gCO_2$-eq/kWh considered in the calculation.

**Table 11.** 3 kV DC link 3-phase inverter details and inverter lifetime energy and $CO_2$-eq savings (25 years) in relation to the 6.5 kV Si IGBT-based inverter.

| Inverter Configuration | Si—2 Level | SiC—3 Level $R_G$: 2.4 Ω | SiC—3 Level $R_G$: 24 Ω |
|---|---|---|---|
| Converter rating [kW] | 788 | 833 | 833 |
| Switching frequency [Hz] | 500 | 1500 | 500 |
| Lifetime energy savings compared to the Si inverter [MWh] | - | 200.7 | 177.9 |
| $CO_2$-eq saved [tons] * | - | 76.5 | 67.8 |

* Carbon intensity generation of 381 $gCO_2$-eq/kWh considered in the calculation.

The converter ratings come from the loadability analysis in Section 5.3.

### *5.6. Financial Analysis*

An investigation of the cost and payback time of substituting Si IGBT with SiC MOSFET inverters is demonstrated in this section. This section estimates the inverter price by considering only the cost of semiconductor modules. Such consideration aims to investigate how the higher initial SiC inverter costs per kWh can be mitigated through the years of operation. It is essential to emphasize that this approach of only considering the power module cost represents a worst-case scenario since the overall converter price comprises several other components (cooling, passive components, PCBs, busbars, etc.). Consequently, the price difference between Si and SiC-based converters is overestimated when only the semiconductor cost is considered. Based on market quotations, the 3.3 kV Silicon IGBT LinPak module costs around 1000 €. Since the SiC LinPak module is not yet available on the market, we assume, based on lower voltage commercial devices, that this module will cost around 3.5 times more than the silicon version, leading to a value of 3500 €. Regarding the 6.5 kV module, based on market quotations, a cost of around 2000 € is expected. Finally, for the 3.3 kV/300 A SiC module, a linear downrating of the 500 A version cost was performed since the device's current rating is directly related to the chip area, leading to a price of

2100 €. The values above are not based on industrial quantities. It is expected that these prices will decrease as companies increase their ordered quantities. The railway electricity cost is based on Germany in 2023, with a price of 13 cents per kWh [40], and France for the same year with a cost of ~47 cents per kWh [41]. Both cases have been considered to evaluate the payback time of SiC in railway inverters. It was considered the cumulative cost per kW of the inverter (accumulated cost over time divided by the inverter nominal power). The inverter initial price (per kW) is estimated from the number of modules used to build the inverter divided by the inverter power rating (Tables 10 and 11). Then, the cumulative price (per kW) over time is calculated based on the yearly average energy losses for each topology configuration.

#### 5.6.1. 1.5 kV DC Link System

Figure 20A shows that for the case of 13 cents per kWh, after 25 years, the cumulative cost of SiC and Si are equalized for the SiC low gate resistance configuration and around 30 years for the SiC high gate resistance case: Both payback times are high, close to the end of the inverter lifetime of about 25 years. However, when considering the case of 47 cents per kWh (Figure 20B), the time required to equalize the cumulative cost is around 7.5 years for both topology configurations with a final cost saving per inverter of around 30 €/kW (30 years lifetime). Both SiC configurations present similar cost savings behavior. The low gate resistance configuration presents slightly better savings and operates at 1.5 kHz, providing a better voltage to the motor and possibly increasing the energy saving from the motor side. This topology requires an output $dv/dt$ filter to protect the motor insulation. Such a filter increases the system size and reduces the overall efficiency. The designer can optimize the filter design according to the most important KPI, focusing more on better efficiency or improved power density. For example, Ref. [12] developed a filter of about 14% of the total inverter weight.

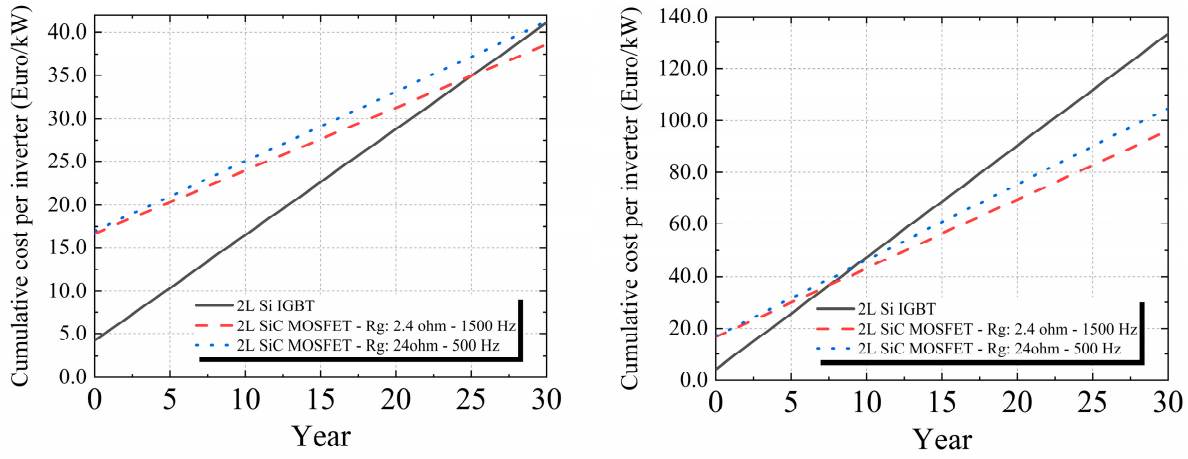



**Figure 20.** Payback time curves per inverter during the inverter's lifetime (1.5 kV DC link). (**A**) Railway electricity cost of 13 cents per kWh. (**B**) Railway electricity cost of 47 cents per kWh.

On the other hand, the option with high gate resistance may not require an output filter depending on the distance between the motor and the inverter. This would be an advantage in terms of system power density. Another fact that can be considered in the cost analysis is the implementation of carbon credit policies by the governments [2], further improving the cost-saving potential of the SiC technology.

5.6.2. 3 kV DC Link System

The same qualitative observations from the 1.5 kV DC case are valid in comparing the different gate resistance configurations. The main difference observed here is that for both energy price cases (Figure 21), the SiC topologies present a faster payback time of around 11 and 3 years for the 13 and 47 cents per kWh cases, respectively. For the 47 cents per kWh case, an impressive cost reduction of around 130 €/kW (30 years lifetime) is obtained. This is an excellent characteristic in favor of using 3.3 kV SiC modules in 3 kV railway systems regarding energy savings (lower carbon footprint) and long-term cost reduction. Naturally, other KPIs like system power density and complexity should be evaluated in the design.

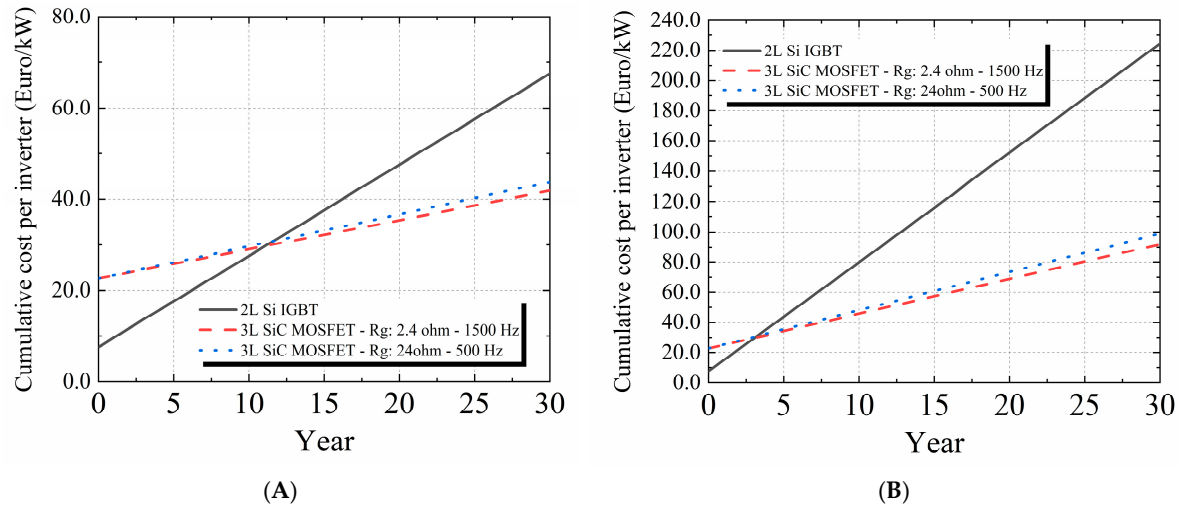



**Figure 21.** Payback time curves per inverter during the inverter's lifetime (3 kV DC link). (**A**) Railway electricity cost of 13 cents per kWh. (**B**) Railway electricity cost of 47 cents per kWh.

## 6. Conclusions

This work performed a systematic comparison of state-of-the-art 3.3- and 6.5-kV Si and SiC power modules for railway traction inverters. Initially, the electrical characteristics of Si and SiC were compared, demonstrating the outstanding performance of SiC at partial-loads and lower temperatures, as well as switching performance under distinct switching speeds. Then, Si and SiC-based power converters were characterized in a dedicated power converter test bench to evaluate both technologies under distinct operational conditions using two accurate loss characterization methods (electrical and calorimetric). Both methods were compared and proved to have a high accuracy. A good understanding of the operational limits was provided for distinct load currents and switching frequencies, showing performance improvements in partial load conditions of ~1.5% in efficiency compared to Si. The switching frequency limits were also investigated, with SiC technology enabling significant increases in switching frequency (>1000 Hz) without aggressively penalizing converter efficiency. Finally, electrothermal models were developed and validated against the experimental results. The developed models demonstrated high accuracy under the tested operating conditions and were suitable for evaluating system performance.

Commercial two- and three-level railway traction topologies with validated electrothermal models were investigated, focusing on 1.5 kV and 3 kV DC link railway systems. The simulation results provided further understanding of the design characteristics, further limiting the possible design configurations to achieve high efficiency and reasonable loadability. Then, drive cycle models were developed, and the energy loss savings from the SiC topologies were evaluated, yielding ~40–70% energy loss savings compared to Si-based topologies. In addition, the drive cycle conditions regarding current level and

temperature operation were evaluated, and the influence on the potential energy savings was discussed. The lifetime energy savings were estimated based on a specific train use pattern over the years, reaching up to 200 MWh in a converter lifetime of 25 years. Furthermore, due to the significant lifetime energy savings, it was estimated that $CO_2$-eq emissions could be reduced by up to ~76 tons per SiC-based inverter. Then, a financial assessment of the proposed topologies was performed. In all energy price scenarios investigated, SiC could mitigate the higher initial converter costs per kW and even save money in the long term. Scenarios with higher energy prices tend to yield faster payback times. The financial analysis was performed based only on the power module cost, which represents a worst-case scenario, since the overall converter price includes several other components at the system level (cooling, passive components, PCBs, busbars, etc.). Consequently, the SiC inverter price difference was overestimated compared to the silicon one. On top of that, further system-level optimizations are possible with SiC (e.g., cooling), which would further improve the SiC inverter's price per kWh. It is also important to mention that the comparison in this paper is based on a well-established Si IGBT technology and a recent SiC module technology (engineering sample). 3.3 kV SiC technology will likely have intensive developments and gain further maturity, improving the performance even more compared to Si IGBT technology. Finally, a discussion on the power converter design parameters (e.g., switching frequency, gate resistance, $dv/dt$) was also provided, focusing on energy savings, financial payback time, and power rating. The results presented aim to provide a detailed investigation of the design possibilities and their effects on key parameters for designers of future SiC-based railway traction systems.

**Author Contributions:** Conceptualization, L.B.S., T.B.S. and R.A.M.; methodology, L.B.S., T.B.S. and R.A.M.; software, L.B.S.; validation, L.B.S. and T.B.; formal analysis, L.B.S.; investigation, L.B.S.; resources, R.A.M.; data curation, L.B.S.; writing—original draft preparation, L.B.S.; writing—review and editing, L.B.S., T.B. and T.B.S.; visualization, L.B.S.; supervision, R.A.M.; project administration, R.A.M.; funding acquisition, R.A.M. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by Swiss Federal Office of Energy (SFOE) under SiC Mile project, grant number SI/502290.

**Data Availability Statement:** The original contributions presented in the study are included in this article; further inquiries can be directed to the corresponding author/s.

**Acknowledgments:** The authors thank Hitachi Energy, Switzerland, for providing state-of-the-art power modules. The authors have reviewed and edited the output and take full responsibility for the content of this publication.

**Conflicts of Interest:** The authors declare no conflicts of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript; or in the decision to publish the results.

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