Passivation Strategies for Minimizing Inversion Leakage in SiC MOS Capacitors.

Rodrigo Reigota César[1], Melissa Mederos Vidal[2], Frederico H. Cioldin[3], Giuliano Maiolini[4], Renato A. Minamisawa[5], Marcos V. Puydinger dos Santos[6], Alexandre Diniz[7]

[1,2,3] Center for Semiconductor Components and Nanotechnology (CCSNano), University of Campinas, Campinas, SP, Brazil,
[4] Renato Archer Information Technology Center (CTI) Campinas, SP, Brazil,
[5] FHNW University of Applied Sciences and Arts Northwestern Switzerland School of Engineering Northwestern Switzerland,
[6,7] Faculty of Electrical and Computer Engineering (FEEC), University of Campinas (UNICAMP), Campinas, SP, Brazil,
e-mail: rorecesa@unicamp.br

Abstract— **In this work, MOS capacitors employing a 50 nm-thick TiO_2 film as the gate dielectric were developed to investigate the effect of different SiC surface passivation strategies. These approaches include an N_2+O_2 plasma treatment of the SiC surface prior to TiO_2 deposition, as well as the insertion of thin SiO_2 interlayers at the TiO_2/SiC interface. Both strategies aim to reduce the leakage current in the capacitors and to passivate the SiC substrate by decreasing the interfacial charge density. In one approach, passivation was carried out using inductively coupled plasma (ICP) at room temperature, while in the other, SiO_2 films with thicknesses of 2 nm and 10 nm were deposited by the PECVD technique between the TiO_2 layer and the SiC substrate. Ellipsometry analysis suggested a deviation from stoichiometry, indicating oxygen-rich SiO_2 films and a titanium-rich TiO_2 film. Raman and FTIR analyses indicated that the TiO_2 film exhibits an anatase crystalline structure. Electrical characterization confirmed that the 2 nm-thick SiO_2 interlayer reduced the device leakage current by two orders of magnitude, although it was ineffective in passivating the SiC surface. In contrast, N_2+O_2 plasma passivation yielded a higher-quality interface, as evidenced by an almost null C–V hysteresis, indicating a significant reduction in trapped charges at the interface.**

Index Terms— **SiC MOS capacitor, TiO_2, Interface Passivation, SiO_2, Leakage Current.**

I. Introduction

Silicon carbide (SiC) has emerged as a highly promising material for the microelectronics industry, owing to its outstanding properties. These include a wide band gap (>2.4 eV), high thermal conductivity, a substantial breakdown field (3.8×10^6 V/cm), and excellent electron saturation velocity (~2×10^7 cm/s) [1-3]. These characteristics make SiC an ideal candidate for power devices operating under extreme conditions, such as those in aerospace, satellite systems, and nuclear reactors [1].

A key advantage of SiC-based metal-oxide-semiconductor (MOS) capacitors is their capability for high-speed switching at elevated voltages, surpassing the performance of conventional silicon devices. This enables higher operating frequencies in integrated circuits and efficient capacitor switching in energy conversion systems [1]. The development of such compact, robust devices is particularly advantageous for space applications, an area of active research for organizations like NASA [2]. Ongoing initiatives are exploring SiC MOS capacitors for use in electric vehicle and aircraft motors, as well as in compact solar panels for clean energy [3]. This collective potential positions SiC as a superior successor to silicon for future high-temperature and high-power electronic devices [1].

Despite these advantages, the performance of SiC devices is hampered by substrate and interface quality. The SiC surface typically exhibits an interface trap density two orders of magnitude higher than that of silicon [1]. These interface charges degrade device performance by reducing carrier mobility in the transistor channel [4]. Consequently, improving the quality of the SiC/gate dielectric interface through effective surface passivation has become a central research focus [5]. In the development of MOS capacitors, the efficacy of these improvements is quantified by minimizing key metrics: capacitance hysteresis (ΔV_{FB}), interface trap density (D_{it}), and, most critically, the gate leakage current density under inversion bias [6]. This leakage current in inversion is the paramount reliability concern for SiC power MOS devices. In a power MOSFET, the inversion layer forms the active conduction channel. A high leakage current in this regime directly compromises channel stability, degrades gate oxide integrity, accelerates time-dependent dielectric breakdown (TDDB), and increases static power loss, thereby adversely impacting the overall efficiency and reliability of the power system [6].

Among various gate dielectrics, titanium dioxide (TiO_2) is noteworthy due to its high dielectric constant (high-κ). Its attractive properties, such as a high refractive index, chemical stability, and hydrogen bonding capability, make it suitable for applications in solar cells, MOS capacitors, and biosensors [6]. TiO_2 exists in three crystalline phases—rutile, anatase, and brookite—each with distinct properties dictated by deposition conditions [6]. The rutile and anatase phases are of particular interest for this study due to their high dielectric constants, which enhance capacitance in MOS capacitors.

However, TiO_2 presents two significant challenges for this application: a relatively narrow band gap and a low conduction band offset with SiC [7]. These properties can lead to increased leakage current, directly exacerbating the core reliability issue described above. A common strategy to mitigate this is to insert a thin SiO_2 layer between the high-κ dielectric and the substrate to act as a potential barrier. Yet, for SiC, this interlayer can itself introduce defects if not optimally thin. An alternative approach is to passivate the SiC surface directly, for example using an N_2+O_2 plasma treatment. This process reduces interface defect density, stabilizes chemical bonds, and improves electrical performance and long-term reliability [7].

Digital Object Identifier 10.29292/jics.v21i1.1140

Based on this context, this study has two primary objectives: first, to evaluate the use of a thin SiO_2 interlayer between TiO_2 and the SiC substrate as a barrier to minimize the critical inversion leakage current; and second, to investigate its role as a passivation layer for improving the TiO_2/SiC interface. The effectiveness of the SiO_2 interlayer will be compared directly with conventional N_2+O_2 plasma passivation. To identify the optimal configuration, two different SiO_2 thicknesses (2 nm and 10 nm) were be analyzed to determine which most effectively enhances the performance and reliability of SiC MOS capacitors for high-power applications.

II. EXPERIMENTAL DETAILS

N-Type 4H-SiC (0001) substrate was utilized to fabricate the devices. Initially, RCA cleaning was performed on all samples. For Sample A, a passivation protocol using inductively coupled plasma (ICP) was performed at room temperature during 20 minutes, with a pressure of 50 mTorr, an RF power of 450 W, and a gas mixture of N_2 (70 sccm) + O_2 (70 sccm).On the other hand, for Samples B and C, SiO_2 layers with thicknesses of 2 nm and 10 nm, respectively, were deposited using the PECVD technique in an Oxford NGP 80 PECVD system. Silane (SiH_4) and nitrous oxide (N_2O) were used as precursors for the deposition. The system featured an 8” heated platen capable of heating the samples to 400°C. The deposition process utilized a gas mixture of SiH_4, N_2O, and N_2, with nitrogen acting as a carrier and diluent for silane. The gas flow rates were set to 5 sccm for SiH_4, 1000 sccm for N_2O, and 1000 sccm for N_2. The process was conducted at a pressure of 2000 mTorr and a temperature of 400°C. A 13.56 MHz RF power supply was employed at 40 W to generate the plasma. To obtain target thicknesses of 2 nm and 10 nm, deposition times were calibrated at 3 seconds and 14 seconds, respectively.

After completing the passivation and the SiO_2 deposition processes, a 50 nm-thick TiO_2 layer was deposited on the top of all the samples (A, B, and C). This deposition was performed using reactive DC sputtering with a power of 1000 W, a 65 sccm argon flow, a 40 sccm oxygen flow, and a deposition time of 10 minutes.

The next step involved optical lithography to define a top circular electrode comprising 800 µm diameter. For this, we use a Durham Magneto Optics MicroWriter ML®3. After lithography, a 150 nm-thick TiN layer was deposited using reactive DC sputtering with a power of 1000 W, a 70 sccm argon flow, and a 20 sccm nitrogen flow for 3 minutes. Then, the samples were immersed in acetone to perform the lift-off process of the TiN, thereby defining the top electrodes for each sample. Next, the native oxide from the bottom surface of each sample was removed and a 300 nm-thick aluminum layer was deposited using a DC sputtering with a power of 1000 W, and a 60 sccm argon flow for 3 minutes. Figure 1 presents the schematic of the three processes (A, B, and C) developed in this work.

Once the capacitor manufacturing was completed, measurements of current versus voltage (I-V) were made using a Keithley 4200 SCS capacitance meter.

The structural properties of the films were monitored using witness samples, which were fabricated concurrently with the devices and characterized by ellipsometry, Fourier-transform infrared spectroscopy (FTIR), Raman spectroscopy, X-ray photoelectron spectroscopy (XPS), and Kelvin probe force microscopy (KPFM).

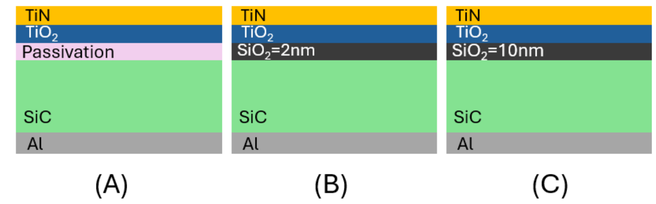

Fig.1. Cross section of each SiC MOS capacitor samples; (A) sample with passivation (N_2+O_2), (B) sample with 2 nm-thick SiO_2 and (C) sample with 10 nm-thick SiO_2.

III. RESULTS AND DISCUSSIONS

A Rudolph Auto-EL II ellipsometry system was employed for ellipsometry analysis, using a 633 nm wavelength and a 70º incident angle. This technique allows for determining film thickness and refractive index (η). The 50 nm thick films exhibited and average thickness of around 50.2 ± 0.5 nm and a refractive index (η) of 2.46 ± 0.02. For reference, the refractive index of stoichiometric TiO_2 is 2.41 [8], thus representing a 2% deviation. Films with a refractive index higher than the stoichiometric value suggest a higher relative Ti concentration [5]. The SiO_2 films of samples B and C exhibited average thicknesses of 2.2 ± 0.5 nm and 10.4 ± 0.5 nm, respectively, with corresponding refractive indices of 1.41 ± 0.02 and 1.43 ± 0.02. The theoretical refractive index of a stoichiometric SiO_2 film is expected to be 1.46, thus indicating that these films are oxygen-rich [8].

To evaluate the effect of plasma passivation on SiC surfaces, KPFM and XPS measurements were performed using a PARK SYSTEMS NX-10 microscope operating in single-pass mode under relative humidity of less than 5% in an N_2 atmosphere and without high vacuum, and using a Pt/Ir coated silicon probe from NanoSensors, model PPP-EFM, with a nominal force constant of 2.8 N/m and a nominal resonance frequency of 75 kHz, and a Thermo Scientific K-Alpha spectrometer equipped with a microfocused Al Kα X-ray source (variable spot size) and a double-focusing hemispherical analyzer with 128-channel detection, respectively. Figure 2 presents the surface potential measured by KPFM for the 4H-SiC substrate and the 4H-SiC substrate after passivation with an N_2+O_2 plasma. The surface potential shows a significant decrease from 565.5 mV to 278.6 mV after passivation. This reduction suggests a decrease in surface electronic states (i.e., fewer surface defects), thus indicating a lower density of trap states that could cause electrical instability. Furthermore, the formation of compounds such as SiO_2 and SiO_xC_γ during the passivation process modified the charge distribution near the surface, enhancing its electrical stability. This interpretation is corroborated by the XPS spectra in Figure 3. The Si 2p region shows an intense peak at 104.5 eV, corresponding to silicon oxide (SiO_2) [9-11], along with peaks at 102 and 101.5 eV, associated with Si–C–O bonds and the formation of SiO_xC_γ structures, respectively. The O 1s region further confirms this assignment, exhibiting a main peak at ~534.0 eV, which is related to Si–O bonds in SiO_2 [9, 12-13].

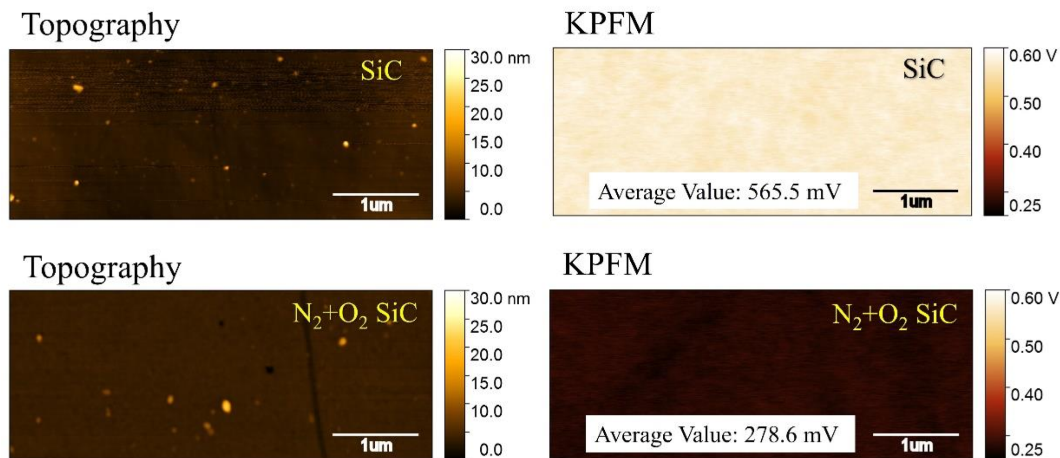

Fig. 2. Surface potential for the 4H-SiC substrate (Top) and the 4H-SiC substrate after passivation with an N_2+O_2 plasma (Bottom), obtained from KPFM measurements.

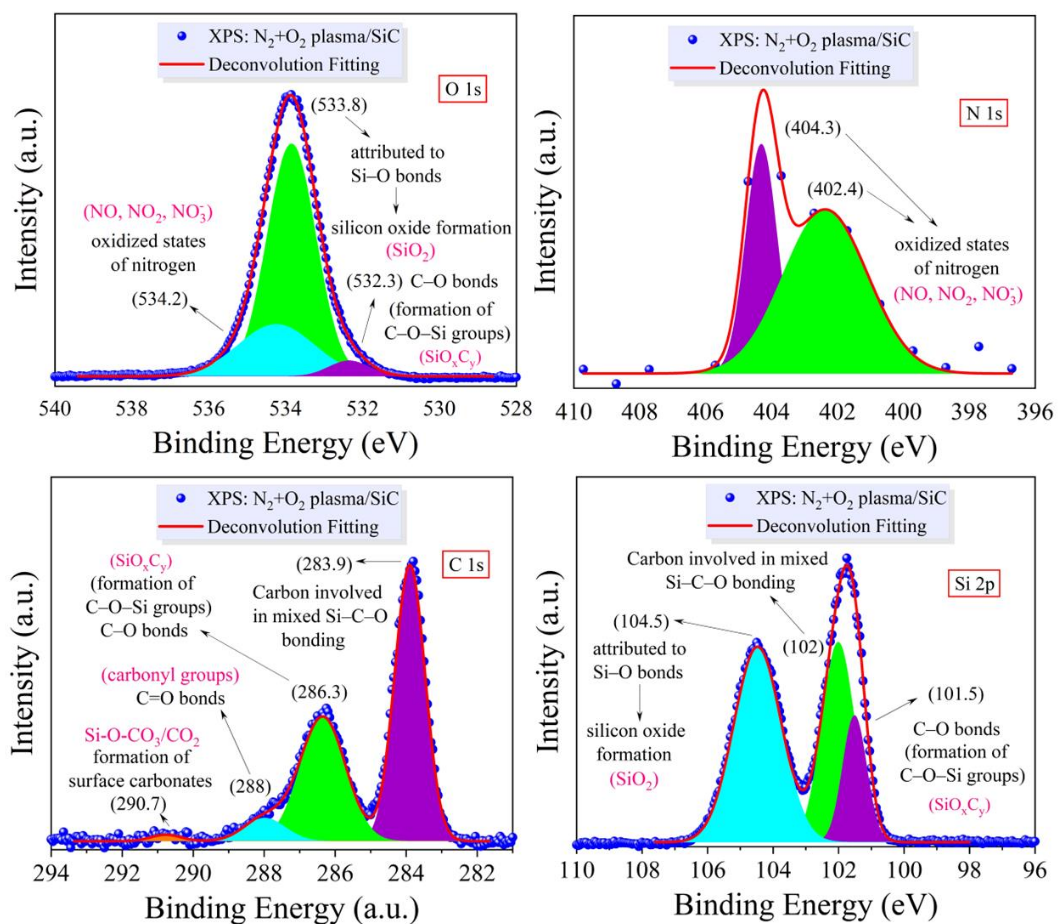

Fig. 3. XPS spectra of 4H-SiC after passivation with N_2+O_2 plasma.

Raman spectroscopy showing in Figure 4, was performed to identify the crystalline phase of TiO_2 deposited on the SiC substrate, using a Horiba XploRa micro Raman spectrometer equipped with a green laser (532 nm) with 15 mW maximum power (100%) and a high-sensitivity CCD detector. The spectrum reveals the characteristic peaks of the anatase phase at 399 cm^{-1} (symmetric mode) and 639 cm^{-1} (characteristic anatase peak), along with characteristic SiC peaks at 206 cm^{-1}, 612 cm^{-1} (related to TO and LO optical photonics modes, respectively), and 197 cm^{-1} (associated with vibrational modes of SiC) [14-16].

Additionally, complementary chemical analysis was performed using FTIR spectroscopy with a Bruker VERTEX 70v vacuum FT-IR spectrometer. The results are presented in Figure 5. This analysis provides a more comprehensive characterization of the TiO_2 film regarding its chemical bonding.

Digital Object Identifier 10.29292/jics.v21i1.1140

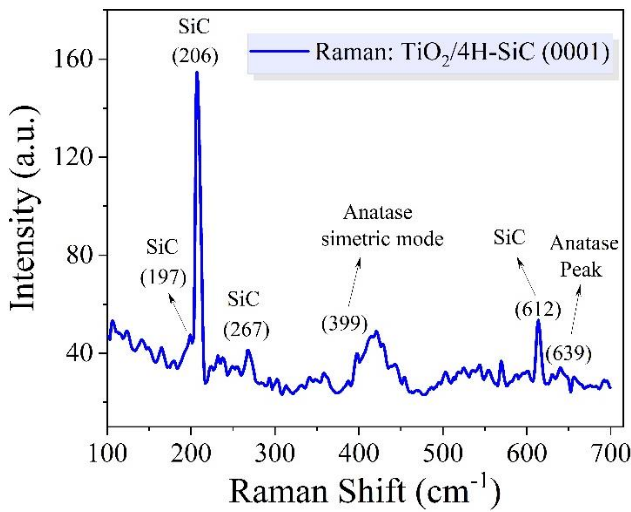

Fig. 4. Raman spectrum of the TiO_2 thin films (TiO_2/SiC), showing the peaks related to the TiO_2 anatase phase.

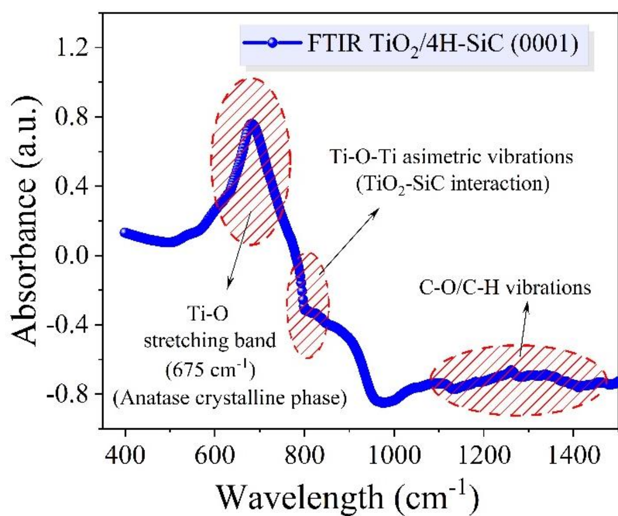

Fig. 5. FTIR spectrum of 50 nm TiO_2 film.

As shown in Figure 5, an absorption band characteristic of the Ti–O bond, associated with the anatase phase, is observed in the 500–700 cm^{-1} region, corresponding to the symmetric and asymmetric stretching vibrations of Ti–O–Ti [14-16]. Additionally, the asymmetric vibrations in the 800-1000 cm^{-1} range are attributed to TiO_2-SiC interactions [14-16]. In the 1200-1400 cm^{-1} region, peaks related to C–O and C–H groups are observed, possibly due to residual organic contamination or adsorption of species during the deposition and treatment process [14-16]. Therefore, based on these analyses, it can be concluded that the crystalline phase of the TiO_2 film is Anatase. Furthermore, for the electrical characterization of the devices, a Keithley 4200 SCS electrometer was used, and current versus voltage (I-V) curves were extracted, with a focus on analyzing the leakage current. Figure 6 presents the I-V curves of the capacitors developed in this work. It is possible to observe that the capacitor subjected to N_2+O_2 plasma passivation (Sample A) demonstrated superior interface quality, evidenced by a hysteresis of ~ 0 V. This indicates a significantly reduced of trapped charges at the interface. The efficacy of this passivation is directly attributed to the chemical modification of the SiC surface, as confirmed by XPS (see Fig. 3) and KPFM analyses (see Fig. 4). The XPS results confirmed the formation of a passivating ultrathin SiO_2 layer and the incorporation of nitrogen in oxidized states, which effectively pacify dangling bonds and defects. This chemical passivation is further quantified by KPFM, which measured a substantial reduction in surface potential on the treated SiC, indicating a decrease in fixed charge at the interface. However, this sample exhibited the highest leakage current in the inversion regime (~10^{-4} A at -5 V). This result confirms that the plasma-grown oxide, while excellent for chemical passivation, is too thin to act as an efficient physical potential barrier against electron injection into the narrow-bandgap TiO_2 gate dielectric.

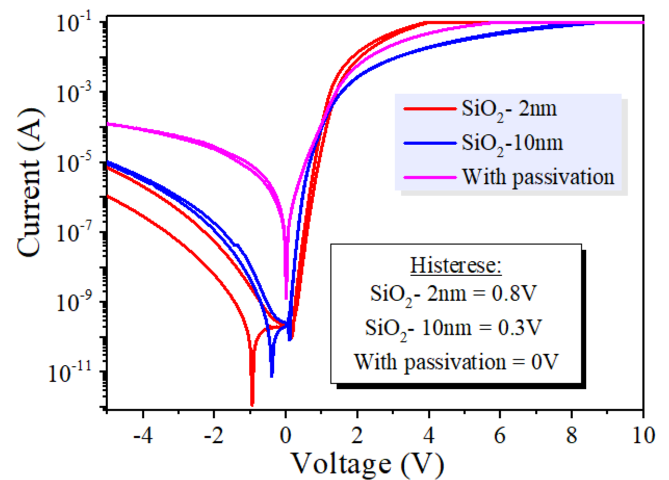

Fig. 6. I-V characteristic curves revealing the leakage current through the SiC MOS capacitor for samples A, B and C.

The capacitor with 10 nm-thick SiO_2 (blue) – sample C – exhibited a hysteresis of 0.3V, indicating the presence of trapped charges at the interface during the capacitor operation cycle between -5 V and 10 V. However, this process resulted in the reduction by one order of magnitude (10^{-5} A) of the leakage current in the inversion regime compared to the passivated sample. In fact, the 10 nm-thick SiO_2 film of sample C is not as effective as sample A with regards to the interface charge passivation, although the additional thick physical barrier can reduce the leakage current, as observed. Therefore, the 10 nm-thick film acts, albeit slightly, as a barrier layer to prevent leakage current.

On the other hand, the capacitor with the 2 nm-thick SiO_2 interlayer (Sample B) presented the most compelling result, highlighting a complex interplay between physical and electrical effects. This device achieved the lowest leakage current in inversion, decreased by two orders of magnitude (~10^{-6} A) compared to the plasma-passivated sample. Paradoxically, it also exhibited the largest hysteresis of 0.8 V. A possible explanation for this result is the following: the thin SiO_2 layer acts as a physical barrier, while the high density of charge traps within it (associated with its oxygen-rich and potentially disordered nature: oxygen-related defects, structural disorder, and residual hydroxyl groups) introduces a significant "electrical" barrier. These traps, with their

characteristic capture and emission time constants, effectively reduce the average current flowing through the MOS structure [17] by immobilizing charge carriers, thereby contributing to the low leakage current despite the poorer interface quality indicated by the large hysteresis.

Therefore, the results delineate a clear design compromise. The N_2+O_2 plasma passivation is optimal for achieving a high-quality interface with minimal trapped charge but fails to mitigate leakage current. Conversely, a deposited SiO_2 interlayer effectively suppresses leakage but degrades interface quality. The 2 nm SiO_2 layer emerged as the most effective barrier, albeit with the highest hysteresis. Based on this understanding, a synergistic approach is proposed for future work: combining the N_2+O_2 plasma passivation to create a superior starting interface with the subsequent deposition of a 2 nm-thick SiO_2 layer to act as an efficient potential barrier. This hybrid strategy is anticipated to simultaneously achieve low interface trap density and low gate leakage, optimizing the overall performance and reliability of SiC-based MOS devices.

CONCLUSIONS

This study successfully evaluated the effectiveness of a SiO_2 interlayer and N_2+O_2 plasma passivation for enhancing the SiC/TiO_2 interface in MOS capacitors. Our findings reveal a fundamental trade-off between interface quality and leakage current suppression. The N_2+O_2 plasma passivation produced a superior electrical interface, as evidenced by the lowest hysteresis value, confirming its role in effective chemical passivation of interface states. However, the resultant ultrathin oxide was insufficient to mitigate the high leakage current inherent to the narrow-bandgap, Ti-rich anatase TiO_2. In contrast, the deposited SiO_2 interlayers, being O-rich, functioned effectively as potential barriers. The 10 nm-thick SiO_2 layer offered a balanced compromise with moderate leakage and hysteresis. Most significantly, the 2 nm SiO_2 interlayer was identified as the optimal configuration for the primary goal of minimizing leakage current in inversion regime, achieving a reduction of two orders of magnitude. This superior barrier effect, however, came at the cost of increased hysteresis, indicating that the ultrathin SiO_2, while an excellent physical barrier, introduces more charge traps than the plasma treatment. Therefore, we conclude that while N_2+O_2 passivation is optimal for interface quality, a 2 nm-thick SiO_2 interlayer is most effective for leakage suppression. For future work, a hybrid approach combining the strengths of both—initial plasma passivation followed by a 2 nm-thick SiO_2 deposition—is proposed to simultaneously achieve a low-trap density interface and a robust leakage barrier.

ACKNOWLEDGEMENTS

Authors would like to thank CCSNano staff for helping in sample preparation and processing. This work was supported by ROTA 2030 (grant #27192-63) and Softex project.

This research used facilities of the Brazilian Nanotechnology National Laboratory (LNNano), part of the Brazilian Centre for Research in Energy and Materials (CNPEM), a private non-profit organization under the supervision of the Brazilian Ministry for Science, Technology, and Innovations (MCTI). The Nanomaterials Division staff (Spectroscopy and Scattering Laboratory and Atomic Force Microscopy Laboratory) is acknowledged for assistance during the experiments (20250233; 20250219; 20250180).

REFERENCES

[1] Langpoklakpam, C., Liu, A. C., Chu, K. H., Hsu, L. H., Lee, W. C., Chen, S. C., Sun, C. W., Shih, M. H., Lee, K. Y., Kuo, H. C., Review of Silicon Carbide Processing for Power MOSFET. Crystals 12 (2022) 245. Available: https://doi.org/10.3390/cryst12020245.

[2] Neudeck, P. G., Spry, D. J., Krasowski, M. J., Chen, L., Greer, L. C., Lukco, D., Beheim, G. M., Prokop, N. F., Upscaling of 500 °C Durable SiC JFET-R Integrated Circuits. Additional Conferences (Device Packaging, HiTEC, HiTEN, and CICMT) (2021). Available: https://doi.org/10.1109/HiTEC.2021.123456.

[3] Afanasev, V. V., Bassler, M., Pensl, G., Schulz, M., Intrinsic SiC/SiO_2 Interface States. Physica Status Solidi A 162 (2001) 321. Available: https://doi.org/10.1002/1521-396X(200107)162:2<321::AID-PSSA321>3.0.CO;2-U.

[4] Nabatame, T., Ohi, A., Chikyo, T., Kimura, M., Yamada, H., Ohishi, T., Electrical properties of anatase TiO2 films by atomic layer deposition and low annealing temperature. Journal of Vacuum Science & Technology B 32 (2014). Available: https://doi.org/10.1116/1.4884213.

[5] César, R. R., Barros, A. D., Doi, I., Diniz, J. A., Swart, J. W., Electrolyte-insulator-semiconductor structure (EIS) with TiO_2 thin film for Pb+ detecting. 31st Symposium on Microelectronics Technology and Devices (SBMicro) (2016) 1–4. Available: https://doi.org/10.1109/SBMicro.2016.7731328.

[6] Dang, V. S., Parala, H., Kim, J. H., Xu, K., Srinivasan, N. B., Edengeiser, E., Havenith, M., Wieck, A. D., Arcos, T., Fischer, R. A., Devi, A., Electrical and optical properties of TiO_2 thin films prepared by plasma-enhanced atomic layer deposition. Physica Status Solidi A 211(2) (2014) 416–424. Available: https://doi.org/10.1002/pssa.201330291.

[7] Sun, Y., Yang, C., Yin, Z., Qin, F., Wang, D., Plasma passivation of near-interface oxide traps and voltage stability in SiC MOS capacitors. Journal of Applied Physics 125 (2019) 185703. https://doi.org/10.1063/1.5093548.

[8] Pliskin, W. A., Esch, R. P., Refractive index of SiO_2 films grown on silicon, Journal of Applied Physics 36 (6) (1965) 2011-2013. Available: https://doi.org/10.1063/1.1714393

[9] Hornetz, B., Michel, H. J., Halbritter, J., ARXPS studies of SiO_2-SiC interfaces and oxidation of 6H SiC single crystal Si-(001) and C-(001) surfaces, Journal of materials research 9 (12) (1994) 3088-3094. Available: https://doi.org/10.1557/JMR.1994.3088

[10] Vidal-Letelier, C., Dorignac, P., Foret, A., Analytical electron tomography mapping of the SiC pore oxidation at the nanoscale, Nanoscale 2 (2010) 1965-1973. DOI: 10.1039/C0NR00449A

[11] Askari, S., Haq, A. U., Macias-Montero, M., Levchenko, I., Yu, F. J., et al., Ultra-small photoluminescent silicon-carbide nanocrystals by atmospheric-pressure plasmas, Nanoscale 8 (2016) 17141-17149. Available: 10.1039/C6NR03702J

[12] Amy, F., Hwu, Y., Brylinski, C., Soukiassian, P., Initial oxidation of the Si-terminated 6H-SiC (0001) 3 × 3 surface, Materials Science Forum 338-342 (2000) 395-398. Available: https://doi.org/10.4028/www.scientific.net/MSF.338-342 .395

[13] Takahashi, S., Hatta, S., Yoshigoe, A., Teraoka, Y., Aruga, T., High-resolution X-ray photoelectron spectroscopy study on initial oxidation of 4H-SiC (0001)-($\sqrt{3} \times \sqrt{3}$) R30° surface, Surface Science 603 (2009) 221-226. Available: DOI.org/10.1016/j.susc.2008.11.005

[14] León, A., et al., FTIR and Raman Characterization of TiO_2 Nanoparticles Coated with Polyethylene Glycol as Carrier for 2-Methoxyestradiol, Applied Sciences 7 (1) (2017) 49 [Online]. Available: https://www.mdpi.com/2076-3417/7/1/49

[15] Sharma, S. K., et al., Electrochemical Processes and Characterization of Doped TiO_2 Thin Films, in Proceedings of the 2009 34th IEEE Photovoltaic Specialists Conference (PVSC), Philadelphia, PA, USA, 2009, pp. 001279-001283. [Online]. Available: https://ieeexplore.ieee.org/document/5336581

[16] Tagantsev, A. K., et al., Preparation and Characterization of TiO_2 Thin Films: A Sol-Gel Approach, in Proceedings of the 2011 International Conference on Nanoscience, Technology and Societal Implications (NSTSI), Bhubaneswar, India, 2011, pp. 1-4. [Online]. Available: https://ieeexplore.ieee.org/document/6167886

[17] Strand, J., Kaviani, M., Gao, D., El-Sayed, A.-M., Afanas'ev, V. V., Shluger, A. L., Intrinsic charge trapping in amorphous oxide films: status and challenges, Journal of Physics: Condensed Matter 30 (23) (2018) 233001. Available: https://doi:10.1088/1361-648X/aac005.